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[TITLE OF INVENTION IN KOREAN] 횡전계형 액정표시장치 및 그 제조 방법

[TITLE OF INVENTION IN ENGLISH] In-Plane Switching mode Liquid Crystal Display Device and Method for fabricating the same

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[PURPORT] We submit application as above under the article 42 of the Patent Law and claim examination to the application under the article 60 of the patent Law.

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[FEES]

[BASIC APPLICATION FEE]	0 pages	38,000	Won
[ADDITIONAL APPLICATION FEE]	129 pages	0	Won
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[DOCUMENT OF ABSTRACT]

[ABSTRACT]

In the present invention, to provide an in-plane switching mode liquid crystal display device having a structure for preventing deteriorating characteristic of view angle due to color shift depending on gray level inversion, by forming a common electrode and a pixel electrode having pattern of one of a circular band shape and a trisectrix shape in a main region of an opening region, contrast ratio can be increased and the view angle can be widen without the color shift in any view point because liquid crystal molecules has a same orientation director. Also, since overlapping portions with a black matrix decrease, the present invention has an advantage that a difference of brightness, which is occurred because of misaligning, can have minimum value.

[REPRESENTATIVE FIGURE]

FIG. 5

[SPECIFICATIONS]

[NAME OF INVENTION]

In-Plane Switching mode Liquid Crystal Display Device and Method for fabricating the same

[BRIEF EXPLANATION OF FIGURES]

FIG. 1 is a cross-sectional view showing a cross-section of a conventional in-plane switching mode liquid crystal display device.

FIG. 2 is a schematic plane view of an array substrate for an in-plane switching mode liquid crystal display device according to the related art.

FIG. 3 is a schematic plane view of an array substrate for an in-plane switching mode liquid crystal display device having multiple domains according to the related art.

FIG. 4 is a view showing characteristic of view angle of an in-plane switching mode liquid crystal display device having multiple domains of a zigzag shape according to the related art.

FIG. 5 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a first exemplary embodiment of the present invention.

FIGs. 6A to 6E are plane views showing 5 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device according to the first exemplary embodiment of the present invention.

FIG. 7 is a schematic plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a second exemplary embodiment of the present invention.

FIGs. 8A to 8E are plane views showing 5 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device according to the second exemplary embodiment of the present invention.

FIG. 9 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a third exemplary embodiment of the present invention.

FIGs. 10A to 10D are plane views showing 4 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to the third exemplary embodiment of the present invention.

FIG. 11 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a fourth exemplary embodiment of the present invention.

FIGs. 12A to 12D are plane views showing 4 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to the fourth exemplary embodiment of the present invention.

FIGs. 13A to 13D are schematic cross-sectional views showing a conventional lift-off process.

FIG. 14 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a fifth exemplary embodiment of the present invention.

FIGs. 15A to 15D are plane views showing processes of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to the fifth exemplary embodiment of the present invention.

FIG. 16 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a sixth exemplary embodiment of the present invention.

FIGs. 17A to 17D are plane views showing processes of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to the sixth exemplary embodiment of the present invention.

FIG. 18 is a view showing a direction of liquid crystal molecules according to gray levels and simulation results of characteristic of brightness due to a structure of electrode of an in-plane switching mode liquid crystal display device according to the present invention.

FIG. 19 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device according to a seventh exemplary embodiment of the present invention.

FIG. 20 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to an eighth exemplary embodiment of the present invention.

FIG. 21 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a ninth exemplary embodiment of the present invention.

FIG. 22 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device according to a tenth exemplary embodiment of the present invention.

FIG. 23 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to an eleventh exemplary embodiment of the present invention.

FIG. 24 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular shape according to a twelfth exemplary embodiment of the present invention.

FIGs. 25A to 25D and 26A to 26D are cross-sectional views taken along the lines XVa-XVa" and XVb-XVb" of FIGs. 15A to 15D, respectively.

* Explanation of major parts in the figures *

110 : a substrate	112 : a gate line
114 : a common line	118 : opening portion
120a : a first common electrode pattern	120b : a second common line pattern
120 : a common electrode	128 : a data line
138a : a first pixel electrode pattern	138b : a second pixel electrode pattern
138 : a pixel electrode	140a : a first outputting line pattern
140b : a second outputting line pattern	141 : a connection line
T : a thin film transistor	P : a pixel region
Cst : a storage capacitor	

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display device, and more particularly, to an in-plane switching mode liquid crystal display device and a method of fabricating the same.

Generally, a liquid crystal display device uses the optical anisotropy and polarization properties of liquid crystal molecules to produce an image. Liquid crystal molecules have a definite orientational alignment as a result of their long, thin shapes. That alignment direction can be controlled by applying an electric field to the liquid crystal molecules.

Thus, by properly controlling the alignment direction of the liquid crystal molecules, the alignment of the liquid crystal molecules is changed. Due to the optical anisotropy, the refraction of incident light depends on the alignment direction of the liquid crystal molecules such that images are displayed.

Recently, since it has high resolution and superiority in displaying moving images, an active matrix type liquid crystal display (AM-LCD, hereinafter, it is referred as to "liquid crystal display device"), in which a thin film transistor and a pixel electrode connected to the thin film transistor are arranged in a matrix shape, came into the spotlight.

Generally, the liquid crystal display device is constituted of a color filter substrate including a common electrode, an array substrate having a pixel electrode, and a liquid crystal layer therebetween. The liquid crystal display device is driven by the electric field vertically induced between the common electrode and the pixel electrode and has a high transmittance and aperture ratio.

However, since the above-mentioned driving method of the liquid crystal display device using the vertical electric field has a poor view angle, an in-plane switching mode liquid crystal display (IPS-LCD) device, which is driven by a horizontal electric field and has a wide view angle, is suggested to resolve the poor view angle of the liquid crystal display device.

FIG. 1 is a cross-sectional view showing a cross-section of a conventional IPS-LCD device.

As shown, an upper substrate 10, referred to as the color filter substrate, and a lower substrate 20, referred to as the array substrate, face and is spaced apart from each other and the liquid crystal layer 30 is interposed between the upper and lower substrates 10 and 20. The common electrode 22 and the pixel electrode 24 are formed on an inner surface of the lower substrate 20.

The liquid crystal layer 30 is driven by the horizontal electric field 26 induced between the common electrode 22 and the pixel electrode 24. Since the liquid crystal molecules in the liquid crystal layer 30 moves by the horizontal electric field, the view angle becomes wider.

For example, when the IPS-LCD device is observed in front side, the view angle has ranges from about 80 to 85 degrees in up-and-down and left-and-right sides from a line vertical to the IPS-LCD panel.

FIG. 2 is a schematic plane view of an array substrate for an IPS-LCD device according to the related art.

As shown, a gate line 40 and a data line 42 cross each other, and a thin film transistor (TFT) T is formed at crossing portion of the gate and data lines 40 and 42. A region formed by crossing is defined as a pixel region P, and the common electrode 44 and the pixel electrode 46 are formed in the pixel region P. A region, in which the liquid crystal molecules are horizontally arranged by the horizontal electric field between the common and pixel electrodes 44 and 46, is defined an opening region I.

In more detail, an outputting line 48 is formed to be connected to the TFT T, and the plurality of pixel electrodes 46 extend from the outputting line 48 in a same direction as the data line 42. A common line 50 is formed along a same direction as the gate line 40 and

spaced apart from the gate line 50. The plurality of common electrodes 44 extend from the common line 50 and are alternately arranged with the plurality of pixel electrodes 46.

For example, when the opening portion I between the common electrode 44 and the pixel electrode 46 is defined as a block, FIG. 2 shows four blocks.

As shown in FIG. 2, the IPS-LCD device is driven by the horizontal electric field induced between the common and pixel electrodes. Thus, it can provide a wider view angle than the LCD device using the vertical electric field.

Recently, to much improve the view angle of the IPS-LCD device, a structure having multiple domains is suggested.

FIG. 3 is a schematic plane view of an array substrate for an in-plane switching mode liquid crystal display device having multiple domains according to the related art. Element explained by FIG. 2 is not explained hereinafter, and characteristic structures are mainly explained. The plurality of pixel electrodes 56 extend from the outputting line 58 and have a zigzag shape. The plurality of common electrodes 54 extend from the common line 60 and have the zigzag shape to be alternately arranged with the plurality of pixel electrodes 56.

And, the liquid crystal molecules between the pixel and common electrodes 56 and 54 are differently arranged from each other to bending portions of the pixel and common electrodes 56 and 54 such that the IPS-LCD device has the multiple domains and an improved view angle.

The outputting line 58 overlaps the common line 60 such that an overlapping portion of the outputting line 58 and the common line 60 forms a storage capacitor Cst. One of the plurality of pixel electrodes 56 is integrated to a drain electrode 62 of the TFT T.

However, since the IPS-LCD device having multiple domains due to the zigzag shape has different orientation directors depending on view points, a problem of color shift occurs and there is a limitation to improve the view angle.

FIG. 4 is a view showing characteristic of view angle of an IPS-LCD device having multiple domains of a zigzag shape according to the related art. The IPS-LCD device has an improved view angle in directions of 90 and 180 degrees, i.e., in right-and-left and up-and-down directions, as illustrated by references "IVa" and "IVb" in FIG. 4. However, the viewing angles are degraded in directions of 45 and 135 degrees, i.e., in diagonal directions, as illustrated by references "IVc" and "IVd" in FIG. 4.

Furthermore, the color shift also occurs depending on the viewing angles or directions.

In more detail, when the voltages applied to the electrodes generate the electric fields between the common and pixel electrodes, the liquid crystal molecules rotate about 45 degrees in accordance with the electric fields. Then, gray inversion occurs due to the rotation of the liquid crystal molecules. Especially, when the IPS-LCD is operated in gray mode, the IPS-LCD produces yellowish color in 45(+45) degrees declination with respect to the liquid crystal polarization because of the optical anisotropy properties of liquid crystal molecules. And the IPS-LCD also produces bluish color in 135(-45) degrees declination with respect to the liquid crystal polarization because of the optical anisotropy properties of the liquid crystal molecules.

[TECHNICAL SUBJECT OF INVENTION]

To resolve these problems, the present invention provides an IPS-LCD device and a method of fabricating the same that prevent decreasing characteristic of view angle due to a phenomenon of color shift depending on gray level inversion.

To achieve the above objects, by forming a common electrode and a pixel electrode having opening portion of a circular band shape and a trisectrix shape, the present invention has same orientation directors at any view points such that prevents the phenomenon of color shift and has an improved view angle.

[CONSTRUCTION AND OPERATION OF INVENTION]

To achieve the above objects, the present invention provides an array substrate form an in-plane switching mode liquid crystal display device comprises a gate line along a first direction; a data line along a second direction crossing the first direction; a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode; a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the common line; and an outputting line being connected to the thin film transistor, and a pixel electrode extending from the outputting line and being alternately arranged to be spaced apart from the common electrode, wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

To achieve the above objects, the present invention provides an array substrate form an in-plane switching mode liquid crystal display device comprises a gate line along a first direction; a data line along a second direction crossing the first direction; a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode; a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the

common line; a connection line extending from the drain electrode; and a pixel electrode being connected to the connection line and being alternately arranged to be spaced apart from the common electrode, wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

It has characteristics that the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region, which is defined by crossing of the gate and data lines, and has an opening portion, and the second common electrode pattern has the circular band shape in the opening portion.

It has characteristics that the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode has a circular band shape in a region between the first and second common electrode patterns, and the second pixel electrode pattern has a circular shape in the second common electrode pattern.

It has characteristics that the outputting line includes a first outputting line pattern, a second outputting line pattern and a connection line, wherein the first and second outputting line patterns along the first direction overlaps the first common electrode pattern, the connection line connects the first and second outputting line pattern to the pixel electrode, and the first outputting line pattern is substantially connected to the thin film transistor.

It has characteristics that first and second overlapping regions between the first common electrode pattern and the first outputting line pattern and between the first common electrode pattern and the second outputting line pattern include an insulating material such that the first and second overlapping regions are defined as a first storage capacitor.

It has characteristics that the second outputting line pattern overlaps a previous gate line, and a third overlapping region between the second outputting line pattern and the

previous gate line includes an insulating material such that the third overlapping region is defined as a second storage capacitor.

It has characteristics that the pixel electrode is formed by a lift-off method, wherein the lift-off method includes a step of forming a photosensitive material pattern and an electrode material covering the photosensitive material pattern and a step of using a region of the electrode material, which is remained by stripping the photosensitive material pattern, as a pattern.

To achieve the above objects, the present invention provides an array substrate form an in-plane switching mode liquid crystal display device comprises a gate line along a first direction; a data line along a second direction crossing the first direction; a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode; a common line along the first direction being spaced apart from the gate line; a connection line extending from the drain electrode; a common electrode of a transparent conductive material connected to the common line and spaced apart from the connection line; and a pixel electrode connected to the connection line, spaced apart from the common line, alternately arranged with the common line to be spaced apart from the common line, and formed of a same material and a same process as the common electrode, wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

It has characteristics that further including a storage capacitor including a previous gate line, a storage electrode and an insulating material, wherein the storage electrode extends

from the connection line to overlap the previous gate line, and the insulating material is interposed between the previous gate line and the storage electrode.

It has characteristics that the common and pixel electrodes are formed by a lift-off method, wherein the lift-off method includes a step of forming a photosensitive material pattern and an electrode material covering the photosensitive material pattern and a step of using a region of the electrode material, which is remained by stripping the photosensitive material pattern, as a pattern.

It has characteristics that the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region and has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion.

It has characteristics that the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode has a circular band shape in a region between the first and second common electrode patterns, and the second pixel electrode pattern has a circular shape in the second common electrode pattern.

It has characteristics that the second pixel electrode is located at a crossing portion of the common line and the connection line.

To achieve the above objects, the present invention provides an array substrate form an in-plane switching mode liquid crystal display device comprises a gate line along a first direction; a common line along the first direction being spaced apart from the gate line; a data line along a second direction crossing the first direction; a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode; a connection line extending from the drain

electrode; a passivation layer having first and second contact holes on the thin film transistor and an entire surface of a substrate, wherein the first contact hole partially exposes the common line, and the second contact hole partially exposes the connection line; a common electrode along the first direction formed on the passivation layer and having an integrated pattern in adjacent pixel regions, wherein the common electrode is connected to the common line through the first contact hole, is formed of a transparent conductive material, and has an opening portion in each pixel region; and a pixel electrode connected to the connection line through the second contact hole on the passivation layer, wherein the pixel electrode is spaced apart from the common electrode in the opening portion of the common electrode and is formed of a same material and a same process as the common electrode, wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes and are formed by a lift-off method.

To achieve the above objects, the present invention provides an array substrate form an in-plane switching mode liquid crystal display device comprises a gate line along a first direction; a data line along a second direction crossing the first direction; a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode; a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the common line; and an outputting line being connected to the thin film transistor, and a pixel electrode extending from the outputting line and being alternately arranged to be spaced apart from the common electrode, wherein the common electrode and the pixel electrode have an aperture region of a trisectrix shape at spacing region between the common and pixel electrodes.

It has characteristics that the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region and has an opening portion, and the second common electrode pattern has the trisectrix shape in the opening portion.

It has characteristics that the outputting line overlaps the first common electrode pattern and an insulating material is interposed between the outputting line and the first common electrode pattern such that the outputting line, the first common electrode pattern and the insulating material constitute a storage capacitor.

It has characteristics that the pixel electrode has the trisectrix shape and surrounds a second common electrode pattern.

It has characteristics that further comprising an insulating material between the outputting line and a previous gate line, wherein the outputting line overlaps a previous gate line such that the outputting line, the previous gate line and the insulating material constitute a storage capacitor.

It has characteristics that the semiconductor layer corresponds to the gate electrode and has an island pattern.

It has characteristics that the semiconductor layer is included in a semiconductor material layer corresponding to the data line, the source electrode and the drain electrode.

It has characteristics that the opening portion has a circular shape.

It has characteristics that the opening portion has a corner.

It has characteristics that a pixel region, which is defined by crossing between the gate line and the data line, has a square shape.

It has characteristics that the pixel region includes one of red, green, blue and white colors, and four pixel regions of red, green, blue and white colors constitute a pixel.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises forming a gate line including a gate electrode and a common line including a common electrode on a substrate by patterning a photosensitive material by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion; forming a gate insulating layer on the gate electrode, the gate line, the common electrode and the common line, and a semiconductor layer corresponding to the gate electrode and having an island pattern by a second mask process; forming a data line, a source electrode and a drain electrode on the semiconductor layer by a third mask process, wherein the data line is formed along a second direction crossing the first direction, and the source electrode extends from the data line and is spaced apart from the drain electrode, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming a passivation layer having a drain contact hole on the thin film transistor by a fourth mask process, the drain contact hole exposing the drain electrode; and forming an outputting line and a pixel electrode on the passivation layer by a fifth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of a circular band shape with the common electrode.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion; forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line; forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming a passivation layer having a drain contact hole on the thin film transistor by a third mask process, the drain contact hole exposing the drain electrode; and forming an outputting line and a pixel electrode on the passivation layer by a fourth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of the circular band shape with the common electrode.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises forming a gate line including a gate electrode and a common line including a common

electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion; forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line; forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a connection line, a storage electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the connection line extends from the drain electrode along the second direction, and the storage electrode extends from the connection line to overlaps a previous gate line, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming a passivation layer on the thin film transistor; forming a photoresist pattern having a first opening portion on the passivation layer, the first opening corresponding to a region between the first and second common electrode patterns and a crossing region between the common line and connection line; etching the passivation layer through the first opening portion using the photoresist pattern as a mask; depositing a transparent conductive material on an entire surface of the substrate including the photoresist pattern; performing a lift-off method the transparent conductive material on the photoresist pattern by stripping the photoresist pattern, wherein the remained transparent conductive material is connected the connection electrode exposed by the

passivation layer; and forming a pixel electrode defining an aperture region with the common electrode, the aperture region having a circular band shape.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises forming a gate line along a first direction and a common line on the substrate by a first mask process, the gate line including the gate electrode and spaced apart from the common line; forming an gate insulating layer on the gate electrode, the gate line and the common line; forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a connection line, a storage electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the connection line extends from the drain electrode along the second direction, and the storage electrode extends from the connection line to overlaps a previous gate line, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming photoresist pattern including first and second opening portions on the thin film transistor and having a circular band shape between the first and second opening portions, wherein the first opening portion is spaced apart from the connection line in a pixel region, and the second opening portion is spaced apart from the common line; removing a part of the gate insulating layer using the photoresist pattern to expose the common line; depositing a transparent conductive material on an entire surface of the substrate including the photoresist pattern; and performing a lift-off method the transparent

conductive material on the photoresist pattern by stripping the photoresist pattern, wherein the remained transparent conductive material is defined as a common electrode and a pixel electrode, wherein the common and pixel electrodes are connected to the common and connection lines, respectively, wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a trisectrix shape in the opening portion; forming a gate insulating layer on the gate electrode, the gate line, the common electrode and the common line, and a semiconductor layer corresponding to the gate electrode and having an island pattern by a second mask process; forming a data line, a source electrode and a drain electrode on the semiconductor layer by a third mask process, wherein the data line is formed along a second direction crossing the first direction, and the source electrode extends from the data line and is spaced apart from the drain electrode, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming a passivation layer having a drain contact hole on the thin film transistor by a fourth mask process, the drain contact hole exposing the drain electrode; and forming an outputting line and a pixel electrode on the passivation layer by a fifth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode

pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of a trisectrix shape with the common electrode.

To achieve the above objects, the present invention provides a method of fabricating an array substrate for an in-plane switching mode liquid crystal display device comprises forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a trisectrix shape in the opening portion; forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line; forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor; forming a passivation layer having a drain contact hole on the thin film transistor by a third mask process, the drain contact hole exposing the drain electrode; and forming an outputting line and a pixel electrode on the passivation layer by a fourth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein

the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of the trisectrix shape with the common electrode.

It has characteristics that the opening portion of the first common electrode pattern has a circular shape.

It has characteristics that the opening portion of the first common electrode pattern has a corner.

It has characteristics that the step of forming the pixel electrode further comprises a step of forming a connection line, wherein the outputting line includes first and second outputting line patterns, and the connection line connects between the first outputting line pattern and the pixel electrode and between the second outputting line pattern and the pixel electrode, wherein the first outputting line pattern is substantially connected to the thin film transistor.

It has characteristics that the first and second outputting line patterns overlap the first common electrode pattern such that the first and second outputting line patterns, the first common electrode pattern and an insulating material constitute a storage capacitor, wherein the insulating material is interposed between the first outputting line pattern and the first common electrode pattern and between the second outputting line pattern and the first common electrode pattern.

It has characteristics that the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode pattern having a circular band shape is located between the firs and second common electrode patterns, and the second pixel electrode pattern having a circular shape is located in the second common electrode pattern.

It has characteristics that the step of forming the pixel electrode includes a step of forming first and second pixel electrode patterns, wherein the first pixel electrode pattern

having a circular band shape is located between the firs and second common electrode patterns, and the second pixel electrode pattern having a circular shape is located in the second common electrode pattern.

It has characteristics that the common electrode includes first and second common electrode pattern groups, wherein the first common electrode pattern group surrounds the pixel region and has an opening portion, wherein the second common electrode pattern has a semicircular band shape in the opening portion.

It has characteristics that the pixel electrode includes first and second pixel electrode pattern groups, wherein the first pixel electrode pattern group has a semicircular band shape is located between the firs and second common electrode pattern groups, wherein the second pixel electrode pattern group is located in the second common electrode pattern group.

It has characteristics that patterns in the first and second common electrode pattern groups and the first and second pixel electrode pattern groups is independent on one another.

It has characteristics that a refractional lithography is used for the second mask process.

It has characteristics that the first common electrode pattern, the outputting line and an insulating material constitute a storage capacitor, wherein the first common electrode pattern overlaps the outputting line, and the insulating material is interposed between the first common electrode pattern and the outputting line.

It has characteristics that the pixel electrode has a trisectrix shape and surrounds the second common electrode pattern.

It has characteristics that the pixel region has a square shape.

It has characteristics that the storage electrode, the previous gate line and an insulating material constitute a storage capacitor, wherein the insulating material is interposed between the storage electrode and the previous gate line

To achieve the above objects, the present invention provides an in-plane switching mode liquid crystal display device comprises a first substrate formed by a fabricating method according to one of claims 27 to 32; a second substrate facing the first substrate; and a liquid crystal layer interposed between the first and second substrates.

It is characteristic that the common and pixel electrodes forms an aperture region one of a circular band shape and a trisectrix shape, and an electric field is horizontally formed between the pixel electrode and the common electrode.

It is characteristic that liquid crystal molecules in the liquid crystal layer have a same orientational directors at any view point.

It is characteristic that the second substrate includes a color filter layer and a black matrix having an opening portion, wherein the color filter layer includes one of red, green and blue colors, and the opening portion corresponds to the pixel region.

It is characteristic that further comprising an insulating layer having a first opening portion between the connection line and the pixel electrode, wherein the opening portion corresponding to the pixel electrode and exposes the connection line.

It is characteristic that further comprising a gate pad, a data pad, a gate pad electrode and a data pad electrode, wherein the gate pad is formed at an end of the gate line, and the data pad is formed at an end of the data line, wherein the gate pad electrode and the data pad electrode are connected to the gate and data pads, respectively, and are formed of a same material as the pixel electrode.

It is characteristic that the insulating layer is interposed between the gate pad and the gate pad electrode and between the data pad and the data pad electrode, wherein the insulating layer includes second and third opening portions, wherein the second and third opening portions expose the gate and data pads, respectively, and the gate pad electrode and the data pad electrode are formed in the second and third opening portions, respectively.

It is characteristic that the common electrode includes first and second common electrode patterns, and the pixel electrode includes first, second and third pixel electrode patterns, wherein the first and second pixel electrode patterns are formed between the first and second common electrode pattern and separated from each other to be symmetrical to the common line, wherein the third pixel electrode pattern is located at a crossing portion of the connection line and the common line in a region of the connection line.

It is characteristic that the step of forming the gate line includes a step of forming a gate pad at an end of the gate line, and the step of forming the data line includes a step of forming a data pad at an end of the data line.

It is characteristic that the step of forming the photoresist pattern includes a step of forming second and third opening portions on the photoresist pattern, wherein the second and third opening portions expose the gate and data pad, respectively.

It is characteristic that the step of etching the passivation layer includes a step of removing the transparent conductive material exposed by the second and third opening portions.

It is characteristic that the gate pad is exposed by etching the gate insulating layer and the passivation layer in the second opening portion, and the data pad is exposed by etching the passivatino layer in the third opening portion.

It is characteristic that the transparent conductive material remained in the second opening portion is the gate pad electrode connected to the gate pad, and the transparent conductive material remained in the third opening portion is the data pad electrode connected to the data pad.

It is characteristic that the opening portion includes first, second and third sub-opening portions, wherein the first and second sub-opening portions are spaced apart from each other to be symmetrical to the common line, and the third sub-opening portion is located at a crossing portion of the connection and common lines in the connection line, wherein the pixel electrode includes first, second and third pixel electrode patterns corresponding to the first, second and third sub-opening portions.

Hereinafter, the present invention is explained in detail with reference to the accompanying drawings.

- a first exemplary embodiment -

A process for fabricating an array substrate for an IPS-LCD device having an electrode of a circular band shape is explained by the first exemplary embodiment. In more detail, a five masks process is used in the first exemplary embodiment. The mask process means a photolithography process in which a layer is patterned using a photosensitive material.

FIG. 5 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a first exemplary embodiment of the present invention.

As shown, a gate line 112 along a first direction is formed on a substrate 110, and a data line 128 along a second direction is formed to cross the gate line 112. A TFT T is formed at crossing portion of the gate and data lines 112 and 128.

A crossing region of the gate and data lines 112 and 128 is defined as a pixel region P, and a pixel electrode 138 and a common electrode 120 are formed in the pixel reigon P. In the first exemplary embodiment, the pixel electrode 138 and the common electrode 120 have a circular pattern such that the IPS-LCD device has a same orientation director of a liquid crsytal molecules at any view points and prevents occuring a phenomenon of color shift at a view point.

In more detail, a common line 114 along the first direction is formed to be spaced apart from the gate line 112, and the common electrode 120 extends from the common line 114. The common electrode 120 in the first exemplary embodiment surrounds the pixel region P and includes a first common electrode pattern 120a and a second common electrode pattern 120b. The first common electrode pattern 120a has an opening portion 118 of a circular shpae, and the second common electrode pattern 120b has a circular band shape that is symmetrical to the common line 114.

And, first and second outputting line patterns 140a and 140b are formed to overlap the first common electrode pattern 120a in the first direction, and a connection line 141 extends from the first and second outputting line pattern 140a and 140b to cross the common line 114. The pixel electrode 138 haivng first and second pixel electrode patterns 138a and 138b extend from the connetion lien 141. The first pixel electrode pattern 138a has the circular band shape in a region between the first and seocnd common electrode patterns 120a and 120b, and the second pixel electrode pattern 138b has the circular shape at crossing portion of the connection and common lines 141 and 114.

The pixel reigon P has multiple domains structure due to the connection and common lines 141 and 114.

It is a characteristic that an overlapping region between the first outputting line pattern 140a and the first common electrode pattern 120a and between the second outputting line pattern 140b and the first common electrode pattern 120a functions as a storage capacitor Cst.

Meanwhile, to prevent deteriorating a horizontal electric field between the first common electrode pattern 120a and the first pixel electrode pattern 138a, the first and seocnd outputting line patterns 140a and 140b have a smaller area than the first common electrode pattern 120a with exposing edges of the first common electrode pattern 120a.

In other words, since the common and pixel electrodes have a structure that provides an opening region and the liquid crsytal molecules are arranged along an isoelectric line perpendicular to the electrodes, the IPS-LCD device according to the first exemplary embodiment has an excellent view angle. Also, the liquid crystal molecules are arranged by the horizontal electric field between the common and pixel electrodes as shown in drawing and the phenomenon of color shift along a diagonal line. A problem of color shift at ± 45 degrees in the conventional IPS-LCD device can be resolved.

FIGs. 6A to 6E are plane views showing 5 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device according to the first exemplary embodiment of the present invention.

FIG. 6A shows a first mask process. In the first mask process, the gate line 112 and the common line 114 along the first direction are formed of a first metal material on the substrate 110. The gate line 112 and the common line 114 are spaced apart from each other.

A patterning step is performed by using a photoresist (PR) pattern. The PR pattern is formed by exposing, developing and removing PR. The PR is a photosensitive material.

The step of forming the gate line 112 includes a step of forming the gate electrode 116extending from the gate line 112.

The step of forming the common line 114 includes a step of forming the common electrode 120 surrounging the pixel region P and including the first common electrode pattern 120a and the second common electrode pattern 120b. The first common electrode pattern 120a has the opening portion 118 of the circular shape, and the second common electrode pattern 120b in the opening portion 118 has the circular band shape.

FIG. 6B shows a step of forming a gate insulating layer (not shown) on the gate line 112 and the common line 114 and a step of forming a semiconductor layer 126 on the gate electrode 116 by a second mask process.

Though not shown in drawning, the semiconductor layer 126 includes an active layer of an intrinsic amorphous silicon material and an ohmic contact layer of an impurity-doped amorphous silicon material.

FIG. 6C shows a step of forming the data line 128 on the substrate 110 including the semiconductor layer 126 usnig a second metal materail by a third mask process. The data line 128 along the second direction cross the gate line 112.

The third mask proces includes a step of forming a source electrode 130 and a drain electrode 132 on the semiconductor layer 126. The source electrode 130 extends from the data line 128, and the drain electrode 132 is separated apart from the source electrode 130. The source and drain electrodes 130 and 132 overlap the semiconductor layer 126. The source and drain electrodes 130 and 132 expose the semiconductor layer 126 such that a channel region "ch" is formed.

The gate electrode 116, the semiconductor layer 126, the source electrode 130 and the drain electrode 132 constitue the TFT T.

FIG. 6D shows a step of forming a passivation layer (not shwon) on the TFT T using an insulating material by a fourth mask process. The passivation layer (not shown) includes a drain contact hole 134 partially exposing the drain electrode 132.

FIG. 6E shows a step of forming an outputtng line 140 and the pixel electrode 138 on the passivation layer using a transparent conductive materail by a fifth mask process. The outputting line 140 is connected to the TFT T, and the pixel electrode 138 has a circular shape.

In more detail, the outputting line 140 includes the first and second outputting line patterns 140a and 140b. The first and second outputting line patterns 140a and 140b along the first direction overlap the first common electrode 120a. The fifth mask process includes a step of forming the connection line 141 cross a center portion of the common line 114 in each pixel region P. The pixel electrode 138 includes the first and second pixel electrode patterns 138a and 138b. The first pixel electrode pattern 138a is located between the first and second common electrode patterns 120a and 120b and has the circular band shape. The second pixel electrode pattern 138b is located at a crossing portion of the common line 114 and the connection line 141 and has the circular shape.

The connection line 141 and the common line 114 cross such that the pixel region P includes multiple domains. Each domain has different alignment from each other. The pixel region P may include four domains. Furthermore, since the IPS-LCD device has a same orientational director of the liquid crsytal molecules at any view point due to the circular shpaes of the pixel and common electrodes 138 and 120, a contrast ratio does not deteriorate.

For example, the transparent conductive material may include one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

- a second exemplary embodiment -

The array substrate for an IPS-LCD device having an electrode of a trisectrix shape and the method of fabricating the same through five masks process are explained by the second exemplary embodiment.

Being different from the first exemplary embodiment, the array substrate for the IPS-LCD device according to the second exemplary embodiment has the common electrode and the pixel electrode connected to the common line and the outputting line, respectively, without connection elements. The IPS-LCD device has the same orientational director of the liquid crystal molecules at any view point.

The trisectrix shape may mean as followings: Assume that a point "O" is located on the circle having a diameter "a". Assume that two points "O" and "Q" is located ends of a chord "OQ" of the circle. Another two points "P" is selected so that distances between the points "Q" and "P" is "b". The points "P" are located on the chord "OQ" and the production of the chord "OQ". When the point "A" rounds the circle, the trisectrix shape means a trace of the points "P". The trisectrix shape may be referred to as limason.

FIG. 7 is a schematic plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a second exemplary embodiment of the present invention.

As shown, there is the common line 214 along the first direction. The first common electrode pattern 220a in the pixel region P is connected to the common line 214. The first common electrode pattern 220a is located at edges of the pixel region and a circular opening potion 218. There is the second common electrode pattern 220b in the opening portion of the first common electrode pattern 220a and has the trisectrix shape. The first and second

common electrode patterns 220a and 220b constitue the common electrode 220, and the common electrode 214 is integrated into the common line 214.

The outputting line 240 and the pixel electrode 238 are formed in the pixel region P. the outputting line 240 is connected to the drain electrode 232 of the TFT T and overlaps the first common electrode pattern 220a to be insulated from the first common electrode pattern 220a. The pixel electrode 238 is connected to the outputting line and has the trisectrix shape such that surrounds the second common electrode pattern 220b. The outputting line 240 is integrated into the pixel electrode 238. the second common electrode pattern 220b and the pixel electrode 238 is space apart from each other and have the trisectrix shape.

In this case, when the outputting line 240 is formed to correspond to the first common electrdoe pattern 220a, the outputting line 240 is located an inner side than the first common electrode pattern 220a to induce the horizontal electric field between the first common electrdoe pattern 220 and the pixel electroe 238. The first common electrode pattern 220a, the outputting line 240 and an insulating material therebetween constitute the storage capacitor Cst.

When the electrodes have the above mentiond structures, opening regions between the two electrodes have the trisectrix shape and the liquid crsytal molecules have a same orientational director at any view point.

FIGs. 8A to 8E are plane views showing 5 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device according to the second exemplary embodiment of the present invention.

FIG. 8A shows a step of forming the gate line 212, the common line 214 and the common electrode 220 on the substrate 210 by a first mask process.

The gate line 212 and the common line 214 are along the same direction and spaced apart from each other. The common electrode 220 is integrated into the common line 214. the common electrode 220 includes the first common electrode pattern 220a and the seocnd common electrode pattern 220b. The first common electode pattern 220a has the opening portion 218 of a circular shape. The second common electrode pattern 220b is located in the opening portion 218 and has the trisectrix shape.

Next, FIG. 8B shows a step of forming the gate insulating layer (not shown) and the semiconductor layer 226 by a second mask process, and FIG. 8C shows a step of forming the gate line 212 and the data line 228 crossing each other by a third mask process.

The third mask process includes a step of forming the source and drain electrodes 230 and 232. The source and drain electrodes 230 and 232 is spaced apart from each other such that the semiconductor layer 226 is exposed and the channel reigon "ch" is formed.

The gate electrode 216, the semiconductor layer 226, the source electrdoe 230 and the drain electrode 232 constitute the TFT T.

FIG. 8D shows a step of forming the passivation layer (not shown), which includes the drain contact hole 234 partially exposing the drain electrode 232, by a fourth mask process, and FIG. 8E shows a step of forming the outputting line 240 and the pixel electrdoe 238 by a fifth mask process. The outputting line 240 is connected to the drain electrode 232 through the drain contact hole 234. The pixel electrode 240 extends from the outputting line 240 and has the trisectrix shape. The pixel electrdoe 240 is spaced apart from and surrounds the second common electrdoe 220b.

- a third exemplary embodiment -

The array substrate for an IPS-LCD device having an electrode of a circular band shape and the method of fabricating the same through four masks process are explained by the third exemplary embodiment.

It is characteristic of the third exemplary embodiment that the semiconductor layer, the data line and the channel region are simultaneously formed such that the fabricating process is reduced.

FIG. 9 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a third exemplary embodiment of the present invention.

As shown, the gate line 312 and the data line 328 cross each other, and the TFT T is formed at the crossing portion of the gate line 312 and the data line 328. The pixel electrode 338 is connected to the TFT T, and the common line 314 along a same direction as the gate line 312 is spaced apart from the gate line 312. The common electrode 320 extends from the common line 314 and is alternately arranged with the common electrode 338. The pixel electrode 338 and the common electrode 320 have the ciruclar band shapes.

The gate electrode 316 extends from the gate line 312, and the source electrode 330 extends from the data line 328. The source and drain electrodes 330 and 332 are separated from each other. The semiconductor material layer 325 corresponds to the data line 328 and the source and drain electrodes 330 and 332. The semiconductor material layer 325 corresponds to the source and drain electrodes 330 and 332 is the semiconductro layer 326 of the TFT T.

Hereinafter, the method of fabricating the IPS-LCD device by the four masks process is explained in more detail referring to drawings.

FIGs. 10A to 10D are plane views showing 4 mask processes of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to the third exemplary embodiment of the present invention.

FIG. 10A shows a step of forming the gate line 312 and the common line 314 on the substrate 310 by a first mask process.

The first mask process includes a step of forming the gate electrode 316 and the common electrode 320. The gate electrode 316 and the common electrode 320 are connected to the gate and common line 312 and 320, respectively. The common electrdoe 320 includes the first and second common electrode patterns 320a and 320b.

FIG. 10B shows a step of forming the semiconductor materail layer 325 and the data line 328 by a second mask process. The gate insulating layer, an intrinsic amorphous silcion material, an impurity-doped amorphous silicon material, and a metal material are sequentially formed on the gate line 312, the gate electrode 316, the common line 314 and the common electrode 320. The intrinsic amorphous silcion material, the impurity-doped amorphous silicon material, and the metal material are patterned by the second mask process such that the semiconductor materail layer 325 and the data line 328 having a same pattern are formed.

The second mask process includes a step of forming the source and drain electrodes 330 and 332. The source electrode 330 extends from the data line 328 and overlaps an end of the gate electrode 316, and the drain electrode 332 is separated from the source electrode 330. The semiconductor material layer 325 has a shape corresponding to the source and drain electrodes 330 and 332 and a regon between the source and drain electrodes 330 and 332.

A diffractional lithography is used for the second mask process.

Althogh no shown in the drawing, the diffractional lithography may be performed as followings. A silicon material layer, which includes the intrinsic amorphous silicon materail layer and the impurity-doped amorphous silicon material layer, and the metal layer are sequentailly deposited. A PR layer having a first thickness is formed on the metal layer. A mask, which has a transmissive area, a half-transmissive area and a blocking area, is disposed over the PR layer, and the lithography is performed. Assuming that the PR layer is a negative type in which an irradiated portion of the PR layer is remained by the lithography. The half-transmissvie area corresponds to the channel region, and the transmissive area corresponds to the source and drain electrodes. And the blocking area corresponds to the other portions. A frist PR pattern and a second PR patterns are formed by developing the PR layer. The first PR pattern has a first thickness and corresponds to the source and drain electrodes. The second PR pattern has a second thickness less than the first thickness and corresponds to the channel region. The PR pattern under the blocking region is completely removed. Next, the first and second PR patterns are removed by ashing such that the silicon material layer corresponding to the channel region is exposed. Then, the impurity-doped amorphous silicon layer is removed using the PR patterns such that the intrinsic amorphous silicon layer is exposed. The intrinsic amorphous silicon layer exposed by the above-mentioned process is defined as the channel region.

The semiconductor material layer 325 overlaps the gate electrode 316, the source electrode 330 and the drain electrode 325 is the semiconductor layer 326. The gate electrode 316, the semiconductor layer 326, the source electrode 330 and the drain electrode 325 constitute the TFT T.

Next, FIG. 10C shows a step of forming the passivation layer (not shown) on the TFT by a third mask process. The passivation layer (not shown) is formed on the TFT by

depositing and patterning an insulating material. The passivation layer (not shown) includes the drain contact hole 334 partially exposing the drain electrode 332. FIG. 10D shows a step of forming the pixel electrode 338 on the passivation layer (not shown). The pixel electrode 338 is connected to the drain electrode 332 through the drain contact hole 334.

In more detail, the third mask process includes a step of forming the first outputting line pattern 304a, the second outputting line pattern 304b and the connection line 341. The first outputting line pattern 304a is substantially connected to the drain electrode 332 and overlaps the firs common electrode pattern 320a. The second outputting line pattern 340b faces the first outputting line pattern 340a and overlaps the first common electrode pattern 320a. The connection line 341 connects the first outputting line pattern 340a with the second outputting line pattern 340b.

The pixel electrode 338 includes forming the first pixel electrode pattern 338a and the second pixel electrode pattern 338b. The first pixel electrode pattern 338a extends from the connection line 341 and is located between the first and second common electrode patterns 320a and 320b. The second pixel electrode pattern 338b is located at an inner side of the second common electrode pattern 320b.

The first and second pixel electrode patterns 338a and 338b constitute the pixel electrode 338. The first and second outputting line patterns 340a and 340b, the connection line 341 and the first and second pixel electrode patterns 338a and 338b are integrated into each other.

The IPS-LCD device according to the third exemplary embodiment is driven by a voltage difference between the common electrode formed by the first mask process and the pixel electrode formed by the fourth mask process.

- a fourth exemplary embodiment -

The array substrate for the IPS-LCD device having the electrode of the trisectrix shape and method of fabricating the same using a four masks process is explained in the fourth exemplary embodiment.

In the fourth exemplary embodiment, the refractional lithography is used for a step of forming the semiconductor layer, the data line and the channel region as the third exemplary embodiment such that the fabricting processes decreases.

FIG. 11 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a fourth exemplary embodiment of the present invention.

As shown, the gate line 412 crosses the data line 428, and the TFT T is formed at the crossing portion of the gate and data lines 412 and 428. The pixel electrode 438 is connected to the TFT T. The common line 414 is parallel to and separated from the gate line 412. the commnon electrode 420 extends from the common line 414 and is alternately arranged with the pixel electrode 438. The pixel and common electrodes 438 and 420 have the trisectrix shape.

The gate electrode 416 extends from the gate line 412. The source electrode 430 extends from the data line 428 and is separated from the drain electrode 432. The semiconductor material layer 425 corresponds to the data line 428 and the source and drain electrodes 430 and 432. The semiconductor material layer 425 corresponding to the source and drain electrodes 430 and 432 is the semiconductor layer 426 of the TFT T.

Hereinafter, a method of the IPS-LCD device having the trisectrix shape through a four masks process referring to drawings.

FIGs. 12A to 12D are plane views showing 4 masks process of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to the fourth exemplary embodiment of the present invention.

FIG. 12A shows a step of forming the gate line 412 and the common line 414 by a first mask process. The gate electrode 416 extends from the gate line 412, and the first and second common electrode patterns 420a and 420b extend from the common line 414. the first common electrode pattern 420a is located in a region surrouding the pixel region P and has the circular opening portion 418. The second common electrode pattern 420b is located in the opening portion 418.

FIG. 12B shows a step of forming the semiconductor material layer 425, the data line 428, the semiconductor layer 426, the source and drain electrodes 430 and 432, and the channel region "ch" on the gate line 412, the common line 414 and the first and second common electrode patterns 420a and 420b by a second mask process.

The gate electrode 416, the semiconductor layer 426, the source electrode 430 and the drain electrode 432 constitute the TFT T.

The refractional lithography is used for this step.

FIG. 12C shows a step of forming a passivation layer (not shown) having the drain contact hole 434 on the TFT. The drain contact hole 434 partially exposes the drain electrode 432.

FIG. 12D shows a step of forming the pixel electrode 438 on the passivation layer. The pixel electrode 438 is connected to the drain electrode 432 through the drain contact hole 434.

In more detail, the process shown in FIG. 12D includes a step of forming the outputting line 440 and the pixel electrode 438. The outputting line 440 is substantially

connected to the drain electrode 432 and corresponds to the first common electrode pattern 420a. The pixel electrode 438 extends from the outputting line 440 and is spaced apart from the second common electrode pattern 420b. The pixel electrode 438 has the trisectrix shape such that surrounds the second common electrode pattern 420b.

Hereinafter, a lift-off method for simplifying a fabricating method of the IPS-LCD device having the electrode of circular band shape is explained.

FIGs. 13A to 13D are schematic cross-sectional views showing a conventional lift-off method.

FIG. 13A shows a step of forming a PR pattern 452 in a second region VIb on the substrate 450 using a photosensitive material. The substrate 450 includes a first region VIa and the second region VIb at periphery of the first region VIa. FIG. 13B shows a step of forming a first pattern material 454 on the PR pattern 452.

The first pattern material 454 may include one of a metal material and a transparent conductive material.

Next, FIG. 13C shows a step of striping the PR pattern 452. At this step, the first pattern material 454 corresponding to the PR pattern 452 is also removed by the lift-off method.

Accordingly, as shown in FIG. 13D, the first pattern materail 454 (of FIG. 13C) remained in the first region VIa (of FIG. 13C) is defined as a first pattern 456.

By the lift-off method, a disired pattern can be easily obtained than a photolithography method.

Hereinafter, a fabricating method of the IPS-LCD device using the lift-off method is explained.

- a fifth exemplary embodiment -

In this exemplary embodiment, a metal material is deposited on the substrate including a PR pattern. The PR pattern and the metal meterial corresponding to the PR pattern are removed by the lift-off method. The common electrode is simultaneously formed as the common line, and the pixel electrode is formed of a transparent conductive material by a third mask process. In other words, the IPS-LCD device according to the fifth exemplary embodiment is manufactured by a 3 masks process.

FIG. 14 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to a fifth exemplary embodiment of the present invention.

As shown, the gate line 512 crosses the data line 528, and the TFT T, which includes the gate electrode 516, the semiconductor layer 526, the source electrode 530 and the drain electrode 532, is formed at a crossing portion of the gate and data lines 512 and 528. The pixel electrode 538 is connected to the TFT T. The common electrode 520 extends from the common line 514 and is alternately arranged with the pixel electrode 538. The pixel and common electrodes 538 and 520 have the circular band shape.

The connection line 533 is formed to be parallel to the gate line 512, and a storage electrode 535 overlaps the gate line 512. The connection line 533 and the storage electrode 535 are integrated into the drain electrode 532.

A gate pad 1310 is formed at an end of the gate line 512, and a data pad 1314 is formed at an end of the data line 528. A gate pad electrode 1318 and a data pad electrode 1320 are connected to the gate and data pad 1310 and 1314, respectively. The gate pad

electrode 1318 and the data pad electrode 1320 are located in first and second opening portions XVIa and XVIb.

The pixel electrode 538 is connected to the drain electrode without additional connection elements by forming three patterns extending from the drain electrode.

In the above-mentioned fourth and fifth mask process, the outputting line incluidng the pixel electrode is connected to the drain electrode through the drain contact hole. However, in this exemplary embodiment, the pixel electrode 538 can be connected to the drain electrode 532 without forming the drain contact hole by the lift-off method.

The semiconductor material layer 525 corresponding to the data line 528, the source electrode 530 and the drain electrode 532 includes the semiconductor layer 526. The semiconductor material layer 525, the data line 528, the source electrode 530 and the drain electrode 532 are formed in a same mask process using the refractional lithography.

The gate line 512, the storage electrode 535 overlapping the gate line 512, and the insulating material interposed therebetween constitute the storage capacitoer Cst.

The common electrode 520 includes the first and second common electrode patterns 520a and 520b. The first common electrode pattern 520a is located in the pixel region P and has the opening portion 518 of the circular shape. The second common electrode pattern 520b is located in the opening portion 518 and has the circular band shape. The pixel electrode 538 is formed by the lift-off method and connected to the connection line 533. The pixel electrode 538 includes third, fourth and fifth pixel electrode patterns 538a, 538aa and 538b. The third and fourth pixel electrode patterns 538a and 538aa are located between the first and second common electrode patterns 520a and 520b to be spaced apart from each other and has an oval shape. The fifth pixel electrode pattern 538b is located at a crossing portion of the common line 514 and a second drain electrode pattern 532b in an inner side of

the second common electrode pattern 520b in an inner side of the second drain electrode pattern 532b. The third, fourth and fifth pixel electrode patterns 538a, 538aa and 538b have independent patterns from each other.

It is characteristic that the pixel electrode 538, the gate pad electrode 1318 and the data pad electrode 1320 are formed by the lift-off method.

FIGs. 15A to 15D are plane views showing processes of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to the fifth exemplary embodiment of the present invention, and FIGs. 25A to 25D and 26A to 26D are cross-sectional views taken along the lines XVa-XVa" and XVb-XVb" of FIGs. 15A to 15D, respectively.

FIGs. 15A, 25A and 26A show a step of forming the gate line 512 and the common line 514 on the substrate 510 by a first mask process. The gate and common lines 512 and 514 are formed along the first direction and spaced apart from each other. The first mask process includes a step of forming the gate pad 1310, the common electrode 520 and the gate electrode 516. The gate pad 1310 is formed at the end of the gate line 512. The common electrode 520 includes the first and second common electrode patterns 520a and 520b. The first common electrode pattern 520a surrounds the pixel region P and has the opening portion 518 of the circular shape. The second common electrode pattern 520b is located in the opening portion 518 and has the circular band shape. The gate electrode 516 in each pixel region P extends from the gate line 512.

FIGs. 15B, 25B and 26B show a step of forming the data line 528, the source electrode 530, the drain electrode 532, the semiconductor material layer 525 and the channel region "ch" using the refractional lithography by a second mask process. The data line 528 is formed along the second direction being perpendicular to the first direction. The source

electrode 530 extends form the data line 528 and is separated from the drain electrode 532. The semiconductor material 525 corresponds to the data line 528 and the source and drain electrodes 530 and 532. The semiconductor material 525, which corresponds to the source and drain electrodes 530 and 532, is defined as the semiconductor layer 526. The channel region "ch" is located between the source and drain electrodes 530 and 532.

The data pad 1314 is formed at the end of the data line 528.

The above-mentioned second mask process is performed after the gate insulating layer 1312, a semiconductor material and a data line material are sequentially formed.

The step of forming the drain electrode 532 includes a step of forming the connection line 533 along the first direction and the storage electrode 535 overlapping the gate line 512. The connection line 533 and the storage electrode 535 are integrated into the drain electrode 532.

FIGs. 15C, 25C and 26C show a step of forming the passivation layer 1316 in the pixel region P, a step of forming a separation region II and a PR pattern 536 for the lift-off method, a step of removing the passivation layer 1316 using the PR pattern 536 as a mask, and a step of depositing a transparent conductive material 537. The PR pattern 536 has the first and second opening portions XVIa and XVIb.

The separation region II is located between the first and second common electrode patterns and does not overlap the common line 514. The separation region II includes first, second and third separation region IIa, IIb and IIc. The first and second separation region IIa and IIb is symetrical to the common line 514. The third separation region IIc is located at a crossing portion of the connection line 533 and the common line 514 in the connection line 533. The separation region II corresponds to regions in which the pixel electrode and the pad electrodes are formed. The transparent conductive material 537 in the first to third

separation region IIa, IIb and IIc and the first and second opening portions XVIa and XVIb is connected to the connection line 533, the gate pad 1310 and the data pad 1314.

The passvation layer 1316 and the gate insulating layer 1312 in the first opening portion XVIa is removed such that the gate pad 1310 is exposed. The passivation layer 1316 in the second opening portion XVIb is removed such that the data pad 1314 is exposed.

The above-mentioned lift-off method is performed as followings. First, the PR is pattern is formed on the substrate and the metal layer is deposited on the PR pattern and the substrate. Then, The PR pattern is stripped such that the metal layer on the PR pattern is removed by the lift-off method. The remained metal layer pattern is defined electrode pattern.

FIGs. 15D, 25D and 26D show a step of forming the pixel electrode 538, the gate pad electrode 1318 and the data pad electrode 1320, respectively. The transparent conductive material is deposited on the PR pattern 536 (of FIG. 15C) and the substrate. The PR pattern is stripped and the transparent conductive material on the PR pattern is removed by the lift-off method. The remained transparent conductive materials corresponds to the pixel electrode 538, the gate pad electrode 1318 and the data pad electrode 1320, respectively.

The pixel electrode 538 is transparent conductive material patterns remained in the first to third separation regions IIa, IIb and IIc (of FIGs. 15D, 25D and 26D). The pixel electrode 538 is located between the first and second common line patterns 520a and 520b. The remained transparent conductive material patterns are separated from each other based on the common line 520. In other words, the pixel electrode 538 includes first to third pixel electrode patterns 538a, 538aa and 538b. The first and second pixel electrode patterns 538a and 538b do not overlap the common line 520. The third pixel electrode pattern 538b is

located in regions of the common line 520 and the connection line 533 in region of the connection line 533.

The gate pad electrode 1318 and the data pad electrode 1320 correspond to transparent conductive material patterns remained in the firs and second opening portions XVIa and XVIb, respectively.

In other words, the gate pad electrode 1318 in the first opening portion XVIa is electrically connected to the gate pad 1310, and the data pad electrode 1320 in the second opening portion XVIb is electrically connected to the data pad 1314.

- a sixth exemplary embodiment -

The array substrate for IPS-LCD device having the trisectrix shape and the method of fabricating the same by the lift-off method through a three masks process is explained by the sixth exemplary embodiment. It is characteristic that the common electrode and the pixel electrode are formed of the transparent conductive material in a same mask process.

FIG. 16 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a sixth exemplary embodiment of the present invention.

As shown, the pixel and common electrodes 638 and 620 having the circular shape are alternately arranged. The pixel electrode 638 is formed of a same process and a same material as the common electrode 620.

In more detail, the pixel and common electrodes 638 and 620 are formed of the transparent conductive material by the lift-off method. The common and pixel electrodes 620 and 638 directly contact with the common line 614 and the connection line 633, respectively. To prevent disconnecting between the common electrode 620 and the

connection electrode 633 and between the pixel electrode 620 and the common line 614, the common electrode 620 has a semicircular shape in an overlapping region between the common electrode 620 and the connection line 633, and the pixel electrode 620 has a semicircular shape in an overlapping region between the pixel electrode 638 and the common line 614. The second pixel electrode pattern 638b at a crossing portion of the connection line 633 and the common line 614 is only formed in a region corresponding to the connection line 633.

FIGs. 17A to 17D are plane views showing processes of fabricating an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to the sixth exemplary embodiment of the present invention.

FIG. 17a shows a step of forming the gate line 612 and the common line 614 separated from each other on the substrate 610 by a first mask process. FIG. 17B shows a step of forming the data line 628, the source electrode 630, the drain electrode 632, the semiconductor material layer 625 and the channel region "ch" using the refractional lithography by a second mask process. The semiconductor material 625 corresponds to the data line 628 and the source and drain electrodes 630 and 632. The semiconductor material 625, which corresponds to the source and drain electrodes 630 and 632, is defined as the semiconductor layer 626. The channel region "ch" is located between the source and drain electrodes 630 and 632.

A gate electrode 616, the semiconductor layer 626, the source electrode 630 and the drain electrode 632 constitute the TFT T.

FIG. 17C shows a step of forming the PR pattern 636 for the lift-off method in the pixel region P. FIG. 17D shows a step of exposing the a portion of the substrate, on which the gate insulating layer is only deposited, and a step of depositing the transparent conductive

material on the PR pattern 636 and the substrate. The protion of the substrate is exposed by removing the gate insulating material exposed by the PR pattern 636 using the PR pattern 636 as a mask.

The common electrode and the pixel electrode will be formed in a separation region III between the PR patterns 636.

FIG. 17D shows a step of the pixel and common electrodes 538 and 642. The PR pattern 635 (of FIG. 17C) is stripped and the transparent conductive material 637 (of FIG. 17C) on the PR pattern is removed by the lift-off method such that the pixel and common electrodes 638 and 642 are formed of the remained transparent conductive material.

The pixel and common electrode 638 and 620 are electrically connected to the connection line 633 and the common line 614, respectively. Since the pixel and common electrodes 638 and 620 are formed by the lift-off method, the pixel electrode 638 has the semicircular shape in an overlapping region between the pixel electrode 638 and the common line 614 and the common electrode 620 has the semicircular shape in an overlapping region between the common electrode 620 and the connection line 633. The second pixel electrode pattern 638b at a crossing portion of the connection line 633 and the common line 614 is only formed in a region corresponding to the connection line 633.

FIG. 18 is a view showing a direction of liquid crystal molecules according to gray levels and simulation results of characteristic of brightness due to a structure of electrode of an in-plane switching mode liquid crystal display device according to the present invention. The simulation is perfomred in a normally black mode.

Initially, zero voltage is applied into the liquid crystal molecules. The applied voltage gradually becomes high. For example, the applied voltage becomes from zero

voltage to ten voltages by two voltages. The gray level is observed. Since the liquid crystal molecules have a same orientational director VII, the view angle is improved.

- a seventh exemplary embodiment -

FIG. 19 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device according to a seventh exemplary embodiment of the present invention and shows one pixel region of the array substrate.

The IPS-LCD device includes two electrodes having the circular shape and the pixel region of a square shape. The two electrodes form the horizontal electric field. The pixel region includes four sub-pixels P_R, P_G, P_B and P_W. The four sub-pixels P_R, P_G, P_B and P_W constitute a pixel P_P. The four sub-pixels PR, PG, PB and PW includes one of red, greeen, blue and black colors.

Generally, since three sub-pixels constitute a pixel, the pixel region of conventional IPS-LCD device has a rectangular shpae. To form a circular electrode for improving the aperture ratio, the pixel region in the present invention has the square shape.

However, the IPS-LCD device according to the present invention is not limited to have the square pixel region of the four sub-pixels.

Although not shown, the IPS-LCD device having the electrodes of the trisectrix shape may have the pixel region having the square shape.

- an eighth exemplary embodiment -

The IPS-LCD device in the eighth exemplary embodiment has a mixing structure of a storage structure explained by the first exemplary embodiment and a previous storage structure.

FIG. 20 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to an eighth exemplary embodiment of the present invention.

As shown, the first and second outputting line patterns 840a and 840b overlaps the first common electrode pattern 820a along the first direction. The first outputting line pattern 840a is connected to the TFT T. The second outputting line pattern 840b partially overlaps a previous gate line 812.

The storage capacitor Cst corresponds to a summary of first and second storage capacitor Cst1 and Cst2. Since a storage capacitor Cst is formed of a mixing structure of a common type and a previous type, effectiveness of the storage capacitor Cst is improved.

- a ninth exemplary embodiment -

The IPS-LCD device in the ninth exemplary embodiment has a mixing structure of a storage structure explained by the second exemplary embodiment and the previous storage structure.

FIG. 21 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a trisectrix shape according to a ninth exemplary embodiment of the present invention.

As shown, the outputting line 940 is formed to overlap the first common electrode pattern 920a along the first direction. The outputting line 940 partially overlap the previous gate line 912.

The storage capacitor Cst corresponds to a summary of first and second storage capacitor Cst1 and Cst2. Since a storage capacitor Cst is formed of a mixing structure of a common type and a previous type, effectiveness of the storage capacitor Cst is improved.

- a tenth exemplary embodiment -

FIG. 22 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device according to a tenth exemplary embodiment of the present invention.

As shown, a black matrix 1054 having an opening portion 1052 is formed on the substrate 1050. The opening portion 1052 corresponds to the pixel region P. A color filter layer 1056 is formed on the opening portion 1052.

Assuming that the circular electrode is formed in a first region Xa, a square electrode is formed in a second region Xb, overlapping regions between the black matrix 554 and the first region Xa and between the black matrix 554 and the second region Xb correspond to third and fourth regions Xc and Xd, respectively, the fourth region Xd is greater than the third region Xc.

In other words, since the circular electrode has a smaller overlapping region than the square electrode, a loss of aperture ration resulted from misalignment of upper and lower substrates decreases. Accordingly, differences of brightness respect to products decreases.

- an eleventh exemplary embodiment -

The IPS-LCD device according to the eleventh exemplary embodiment has a common electrode pattern of opening portion shape and an outputting line pattern overlapping the common electrode pattern to improve the aperture ratio.

FIG. 23 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular band shape according to an eleventh exemplary embodiment of the present invention.

As shown, the first common electrode the first common electrode pattern 1120a having an opening portion 1118 surrounds the pixel region P. The opening portion 1118 has a corner portion. The first and second outputting line patterns 1140a and 1140b overlaps the first common electrode pattern 1120 to be along the first direction.

The first common electrode pattern 1120 is connected to the common line 1114. The common line 1114 is across the pixel region P and has the first direction. The connection line 1141 extends from the first and second outputting line patterns 1140a and 1140b and crosses the common line 1114 at the pixel region P. The second common electrode pattern 1120b extends from the common line 1114. The first pixel electrode pattern 1138a extends from the connection line 1141 and surrounds the second common electrode pattern 1120b. The second pixel electrode pattern 1138b is formed in the second common electrode pattern 1120b and has the circular shape.

In the exemplary embodiment, the opening portion 1118 of the first common electrode pattern 1120a has the corner portion corresponding to the pixel region P. Thus, aperture ration becomes greater than in case of the opening portion having circular shape.

Moreover, since the IPS-LCD device according to the exemplary embodiment has the normally black mode, there is no problem of brightness in black color. Brightness is improved due to the corner portion.

Although not shown, the opening portion having the corner may be applied into the IPS-LCD device having the electrode of trisectrix shape.

- a twelfth exemplary embodiment -

The IPS-LCD device having the common electrode and data line overlapping each other is explained by the twelfth exemplary embodiment. The IPS-LCD device has a high aperture ratio.

FIG. 24 is a plane view of an array substrate for an in-plane switching mode liquid crystal display device having an electrode of a circular shape according to a twelfth exemplary embodiment of the present invention.

As shown, the common electrode 1220 and the pixel electrode 1238 are alternately arranged to be separated from each other. The common electrode 1220 and the pixel electrode 1238 have the circular shape. The common electrode 1220 has the opening portion 1218 of circular shape in the pixel region P. The common electrode 1220 includes the first and second common electrode patterns 1220a and 1220b. The first common electrode pattern 1220a has the first direction, and the second common electrode pattern 1220b has the circular band shape in the opening portion 1218. The pixel electrode 1238 includes the first and second pixel electrode patterns 1238a and 1238b. The first pixel electrode pattern 1238a is located between the first and second common electrode patterns 1220a and 1220b. The second pixel electrode 1238b is located in the second common electrode pattern 1220b. In other words, the second pixel electrode 1238b is located at a crossing portion of the drain electrode 1232 and the common line 1214.

The pixel electrode 1238 is formed of a same material and a same process as the common electrode 1220.

The passivation layer is formed between the data line 1228 and the common electrode 1220. The passivation layer includes first and second contact holes 1244 and 1246 and has a low dielectric constant. The common electrode 1220 is connected to the common

line 1214 through the first contact hole 1244, and the pixel electrode 1238 is connected to the drain electrode 1232 through the second contact hole 1246.

Since the interference between the electrodes decreases due to the passivation layer having the low dielectric constant, the common electrode has a great area and the aperture ration is improved.

The pixel electrode is formed of the same material and the same process as the common electrode by a third mask process, and the passivation layer having the low dielectric constant is interposed between the common electrode and the data line.

The passivation layer may include BCB.

Although not shown, the above-mentioned embodiment may be applied into the IPS-LCD device having the circular electrode.

It will be apparent to those skilled in the art that various modifications and variations can be made in the fabrication and application of the present invention without departing from the spirit or scope of the invention.

[EFFECT OF INVENTION]

In the present invention, since the common and pixel electrodes are formed so that the aperture region has the circular shape. Thus, the liquid crystal molecules have the same orientational director such that contrast ration is improved without color shift and the view angle is improved. Moreover, since the overlapping region with the black matrix decreases, the difference of brightness is reduced.

[RANGE OF CLAIMS]

[CLAIM 1]

An array substrate form an in-plane switching mode liquid crystal display device, comprising:

a gate line along a first direction;

a data line along a second direction crossing the first direction;

a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the common line; and

an outputting line being connected to the thin film transistor, and a pixel electrode extending from the outputting line and being alternately arranged to be spaced apart from the common electrode,

wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

[CLAIM 2]

An array substrate form an in-plane switching mode liquid crystal display device, comprising:

a gate line along a first direction;

a data line along a second direction crossing the first direction;

a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the common line;

a connection line extending from the drain electrode; and

a pixel electrode being connected to the connection line and being alternately arranged to be spaced apart from the common electrode,

wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

[CLAIM 3]

The array substrate of claim 1, wherein the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region, which is defined by crossing of the gate and data lines, and has an opening portion, and the second common electrode pattern has the circular band shape in the opening portion.

[CLAIM 4]

The array substrate of one of claims 1 and 3, wherein the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode has a circular band shape in a region between the first and second common electrode patterns, and the second pixel electrode pattern has a circular shape in the second common electrode pattern.

[CLAIM 5]

The array substrate of one of claims 1 and 3, wherein the outputting line includes a first outputting line pattern, a second outputting line pattern and a connection line, wherein the first and second outputting line patterns along the first direction overlaps the first common

electrode pattern, the connection line connects the first and second outputting line pattern to the pixel electrode, and the first outputting line pattern is substantially connected to the thin film transistor.

[CLAIM 6]

The array substrate of claim 5, wherein first and second overlapping regions between the first common electrode pattern and the first outputting line pattern and between the first common electrode pattern and the second outputting line pattern include an insulating material such that the first and second overlapping regions are defined as a first storage capacitor.

[CLAIM 7]

The array substrate of one of claims 5 and 6, wherein the second outputting line pattern overlaps a previous gate line, and a third overlapping region between the second outputting line pattern and the previous gate line includes an insulating material such that the third overlapping region is defined as a second storage capacitor.

[CLAIM 8]

The array substrate of claim 2, wherein the pixel electrode is formed by a lift-off method, wherein the lift-off method includes a step of forming a photosensitive material pattern and an electrode material covering the photosensitive material pattern and a step of using a region of the electrode material, which is remained by stripping the photosensitive material pattern, as a pattern.

[CLAIM 9]

An array substrate form an in-plane switching mode liquid crystal display device, comprising:

a gate line along a first direction;

a data line along a second direction crossing the first direction;

a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a common line along the first direction being spaced apart from the gate line;

a connection line extending from the drain electrode;

a common electrode of a transparent conductive material connected to the common line and spaced apart from the connection line; and

a pixel electrode connected to the connection line, spaced apart from the common line, alternately arranged with the common line to be spaced apart from the common line, and formed of a same material and a same process as the common electrode,

wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

[CLAIM 10]

The array substrate of claim 9, further including a storage capacitor including a previous gate line, a storage electrode and an insulating material, wherein the storage electrode extends from the connection line to overlap the previous gate line, and the insulating material is interposed between the previous gate line and the storage electrode.

[CLAIM 11]

The array substrate of claim 9, wherein the common and pixel electrodes are formed by a lift-off method, wherein the lift-off method includes a step of forming a photosensitive material pattern and an electrode material covering the photosensitive material pattern and a step of using a region of the electrode material, which is remained by stripping the photosensitive material pattern, as a pattern.

[CLAIM 12]

The array substrate of claim 9, wherein the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region and has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion.

[CLAIM 13]

The array substrate of claim 12, wherein the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode has a circular band shape in a region between the first and second common electrode patterns, and the second pixel electrode pattern has a circular shape in the second common electrode pattern.

[CLAIM 14]

The array substrate of claim 13, wherein the second pixel electrode is located at a crossing portion of the common line and the connection line.

[CLAIM 15]

An array substrate form an in-plane switching mode liquid crystal display device, comprising:

a gate line along a first direction;

a common line along the first direction being spaced apart from the gate line;

a data line along a second direction crossing the first direction;

a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a connection line extending from the drain electrode;

a passivation layer having first and second contact holes on the thin film transistor and an entire surface of a substrate, wherein the first contact hole partially exposes the common line, and the second contact hole partially exposes the connection line;

a common electrode along the first direction formed on the passivation layer and having an integrated pattern in adjacent pixel regions, wherein the common electrode is connected to the common line through the first contact hole, is formed of a transparent conductive material, and has an opening portion in each pixel region; and

a pixel electrode connected to the connection line through the second contact hole on the passivation layer, wherein the pixel electrode is spaced apart from the common electrode in the opening portion of the common electrode and is formed of a same material and a same process as the common electrode,

wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes and are formed by a lift-off method.

[CLAIM 16]

An array substrate form an in-plane switching mode liquid crystal display device, comprising:

a gate line along a first direction;

a data line along a second direction crossing the first direction;

a thin film transistor being formed at a crossing portion of the gate and data line and including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a common line along the first direction being spaced apart from the gate line, and a common electrode extending from the common line; and

an outputting line being connected to the thin film transistor, and a pixel electrode extending from the outputting line and being alternately arranged to be spaced apart from the common electrode,

wherein the common electrode and the pixel electrode have an aperture region of a trisectrix shape at spacing region between the common and pixel electrodes.

[CLAIM 17]

The array substrate of claim 16, wherein the common electrode includes first and second common electrode patterns, wherein the first common electrode surrounds a pixel region and has an opening portion, and the second common electrode pattern has the trisectrix shape in the opening portion.

[CLAIM 18]

The array substrate of one of claims 16 and 17, wherein the outputting line overlaps the first common electrode pattern and an insulating material is interposed between the

outputting line and the first common electrode pattern such that the outputting line, the first common electrode pattern and the insulating material constitute a storage capacitor.

[CLAIM 19]

The array substrate of one of claims 16 and 17, wherein the pixel electrode has the trisectrix shape and surrounds a second common electrode pattern.

[CLAIM 20]

The array substrate of claim 18, further comprising an insulating material between the outputting line and a previous gate line, wherein the outputting line overlaps a previous gate line such that the outputting line, the previous gate line and the insulating material constitute a storage capacitor.

[CLAIM 21]

The array substrate of one of claims 1 and 16, wherein the semiconductor layer corresponds to the gate electrode and has an island pattern.

[CLAIM 22]

The array substrate one of claims 1, 2, 9, 15 and 16, wherein the semiconductor layer is included in a semiconductor material layer corresponding to the data line, the source electrode and the drain electrode.

[CLAIM 23]

The array substrate of one of claims 3, 12 and 17, wherein the opening portion has a circular shape.

[CLAIM 24]

The array substrate of one of claims 3, 12 and 17, wherein the opening portion has a corner.

[CLAIM 25]

The array substrate of one of claims 1, 2, 9, 15 and 16, wherein a pixel region, which is defined by crossing between the gate line and the data line, has a square shape.

[CLAIM 26]

The array substrate of claim 25, wherein the pixel region includes one of red, green, blue and white colors, and four pixel regions of red, green, blue and white colors constitute a pixel.

[CLAIM 27]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by patterning a photosensitive material by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern

surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion;

forming a gate insulating layer on the gate electrode, the gate line, the common electrode and the common line, and a semiconductor layer corresponding to the gate electrode and having an island pattern by a second mask process;

forming a data line, a source electrode and a drain electrode on the semiconductor layer by a third mask process, wherein the data line is formed along a second direction crossing the first direction, and the source electrode extends from the data line and is spaced apart from the drain electrode, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming a passivation layer having a drain contact hole on the thin film transistor by a fourth mask process, the drain contact hole exposing the drain electrode; and

forming an outputting line and a pixel electrode on the passivation layer by a fifth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of a circular band shape with the common electrode.

[CLAIM 28]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed

along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion;

forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line;

forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming a passivation layer having a drain contact hole on the thin film transistor by a third mask process, the drain contact hole exposing the drain electrode; and

forming an outputting line and a pixel electrode on the passivation layer by a fourth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of the circular band shape with the common electrode.

[CLAIM 29]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a circular band shape in the opening portion;

forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line;

forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a connection line, a storage electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the connection line extends from the drain electrode along the second direction, and the storage electrode extends from the connection line to overlaps a previous gate line, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming a passivation layer on the thin film transistor;

forming a photoresist pattern having a first opening portion on the passivation layer, the first opening corresponding to a region between the first and second common electrode patterns and a crossing region between the common line and connection line;

etching the passivation layer through the first opening portion using the photoresist pattern as a mask;

depositing a transparent conductive material on an entire surface of the substrate including the photoresist pattern;

performing a lift-off method the transparent conductive material on the photoresist pattern by stripping the photoresist pattern, wherein the remained transparent conductive material is connected the connection electrode exposed by the passivation layer; and

forming a pixel electrode defining an aperture region with the common electrode, the aperture region having a circular band shape.

[CLAIM 30]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line along a first direction and a common line on the substrate by a first mask process, the gate line including the gate electrode and spaced apart from the common line;

forming an gate insulating layer on the gate electrode, the gate line and the common line;

forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a connection line, a storage electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the

data line, and the drain electrode is spaced apart from the source electrode, wherein the connection line extends from the drain electrode along the second direction, and the storage electrode extends from the connection line to overlaps a previous gate line, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming photoresist pattern including first and second opening portions on the thin film transistor and having a circular band shape between the first and second opening portions, wherein the first opening portion is spaced apart from the connection line in a pixel region, and the second opening portion is spaced apart from the common line;

removing a part of the gate insulating layer using the photoresist pattern to expose the common line;

depositing a transparent conductive material on an entire surface of the substrate including the photoresist pattern; and

performing a lift-off method the transparent conductive material on the photoresist pattern by stripping the photoresist pattern, wherein the remained transparent conductive material is defined as a common electrode and a pixel electrode, wherein the common and pixel electrodes are connected to the common and connection lines, respectively,

wherein the common electrode and the pixel electrode have an aperture region of a circular band shape at spacing region between the common and pixel electrodes.

[CLAIM 31]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a trisectrix shape in the opening portion;

forming a gate insulating layer on the gate electrode, the gate line, the common electrode and the common line, and a semiconductor layer corresponding to the gate electrode and having an island pattern by a second mask process;

forming a data line, a source electrode and a drain electrode on the semiconductor layer by a third mask process, wherein the data line is formed along a second direction crossing the first direction, and the source electrode extends from the data line and is spaced apart from the drain electrode, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming a passivation layer having a drain contact hole on the thin film transistor by a fourth mask process, the drain contact hole exposing the drain electrode; and

forming an outputting line and a pixel electrode on the passivation layer by a fifth mask process, wherein the outputting line is connected to the drain electrode and overlaps the first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of a trisectrix shape with the common electrode.

[CLAIM 32]

A method of fabricating an array substrate for an in-plane switching mode liquid crystal display device, comprising:

forming a gate line including a gate electrode and a common line including a common electrode on a substrate by a first mask process, wherein the gate line is formed along a first direction, the common electrode includes first and second common electrode patterns, wherein the first common electrode pattern surrounding a pixel region has an opening portion, and the second common electrode pattern has a trisectrix shape in the opening portion;

forming an gate insulating layer on the gate electrode, the gate line, the common electrode and the common line;

forming a data line along a second direction crossing the first direction, a source electrode, a drain electrode, a semiconductor material layer and a channel by a second mask process, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode, wherein the semiconductor material layer corresponds to the data line, the source electrode and the drain electrode and includes a semiconductor layer corresponding to the source and drain electrodes, and the channel of an intrinsic amorphous silicon is formed between the source and drain electrodes, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode constitute a thin film transistor;

forming a passivation layer having a drain contact hole on the thin film transistor by a third mask process, the drain contact hole exposing the drain electrode; and

forming an outputting line and a pixel electrode on the passivation layer by a fourth mask process, wherein the outputting line is connected to the drain electrode and overlaps the

first common electrode pattern, and the pixel electrode extends from the outputting line, wherein the pixel electrode is spaced apart from the second common electrode pattern in the opening portion and forms an aperture region of the trisectrix shape with the common electrode.

[CLAIM 33]

The method of one of claims 27, 28, 29, 31, 32, wherein the opening portion of the first common electrode pattern has a circular shape.

[CLAIM 34]

The method of one of claims 27, 28, 29, 31, 32, wherein the opening portion of the first common electrode pattern has a corner.

[CLAIM 35]

The method of one of claims 27 and 28, wherein the step of forming the pixel electrode further comprises a step of forming a connection line, wherein the outputting line includes first and second outputting line patterns, and the connection line connects between the first outputting line pattern and the pixel electrode and between the second outputting line pattern and the pixel electrode, wherein the first outputting line pattern is substantially connected to the thin film transistor.

[CLAIM 36]

The method of claim 35, wherein the first and second outputting line patterns overlap the first common electrode pattern such that the first and second outputting line patterns, the

first common electrode pattern and an insulating material constitute a storage capacitor, wherein the insulating material is interposed between the first outputting line pattern and the first common electrode pattern and between the second outputting line pattern and the first common electrode pattern.

[CLAIM 37]

The method of claim 35, wherein the pixel electrode includes first and second pixel electrode patterns, wherein the first pixel electrode pattern having a circular band shape is located between the firs and second common electrode patterns, and the second pixel electrode pattern having a circular shape is located in the second common electrode pattern.

[CLAIM 38]

The method of claim 29, wherein the step of forming the pixel electrode includes a step of forming first and second pixel electrode patterns, wherein the first pixel electrode pattern having a circular band shape is located between the firs and second common electrode patterns, and the second pixel electrode pattern having a circular shape is located in the second common electrode pattern.

[CLAIM 39]

The method of claim 30, wherein the common electrode includes first and second common electrode pattern groups, wherein the first common electrode pattern group surrounds the pixel region and has an opening portion, wherein the second common electrode pattern has a semicircular band shape in the opening portion.

[CLAIM 40]

The method of claim 39, wherein the pixel electrode includes first and second pixel electrode pattern groups, wherein the first pixel electrode pattern group has a semicircular band shape is located between the firs and second common electrode pattern groups, wherein the second pixel electrode pattern group is located in the second common electrode pattern group.

[CLAIM 41]

The method of one of claims 39 and 40, wherein patterns in the first and second common electrode pattern groups and the first and second pixel electrode pattern groups is independent on one another.

[CLAIM 42]

The method of one of claims 28, 29, 30 and 32, wherein a refractional lithography is used for the second mask process.

[CLAIM 43]

The method one of claims 31 and 32, wherein the first common electrode pattern, the outputting line and an insulating material constitute a storage capacitor, wherein the first common electrode pattern overlaps the outputting line, and the insulating material is interposed between the first common electrode pattern and the outputting line.

[CLAIM 44]

The method one of claims 31 and 32, wherein the pixel electrode has a trisectrix shape and surrounds the second common electrode pattern.

[CLAIM 45]

The method one of claims 27 to 32, wherein the pixel region has a square shape.

[CLAIM 46]

The method one of claims 29 and 30, wherein the storage electrode, the previous gate line and an insulating material constitute a storage capacitor, wherein the insulating material is interposed between the storage electrode and the previous gate line

[CLAIM 47]

An in-plane switching mode liquid crystal display device, comprising:

a first substrate formed by a fabricating method according to one of claims 27 to 32;

a second substrate facing the first substrate; and

a liquid crystal layer interposed between the first and second substrates.

[CLAIM 48]

The device of claim 47, wherein the common and pixel electrodes forms an aperture region one of a circular band shape and a trisectrix shape, and an electric field is horizontally formed between the pixel electrode and the common electrode.

[CLAIM 49]

The device of claim 48, wherein liquid crystal molecules in the liquid crystal layer have a same orientational directors at any view point.

[CLAIM 50]

The device of claim 47, wherein the second substrate includes a color filter layer and a black matrix having an opening portion, wherein the color filter layer includes one of red, green and blue colors, and the opening portion corresponds to the pixel region.

[CLAIM 51]

The device of claim 2, further comprising an insulating layer having a first opening portion between the connection line and the pixel electrode, wherein the opening portion corresponding to the pixel electrode and exposes the connection line.

[CLAIM 52]

The device of claim 2, further comprising a gate pad, a data pad, a gate pad electrode and a data pad electrode, wherein the gate pad is formed at an end of the gate line, and the data pad is formed at an end of the data line, wherein the gate pad electrode and the data pad electrode are connected to the gate and data pads, respectively, and are formed of a same material as the pixel electrode.

[CLAIM 53]

The device of one of claims 51 and 52, wherein the insulating layer is interposed between the gate pad and the gate pad electrode and between the data pad and the data pad electrode, wherein the insulating layer includes second and third opening portions, wherein

the second and third opening portions expose the gate and data pads, respectively, and the gate pad electrode and the data pad electrode are formed in the second and third opening portions, respectively.

[CLAIM 54]

The device of claim 2, wherein the common electrode includes first and second common electrode patterns, and the pixel electrode includes first, second and third pixel electrode patterns, wherein the first and second pixel electrode patterns are formed between the first and second common electrode pattern and separated from each other to be symmetrical to the common line, wherein the third pixel electrode pattern is located at a crossing portion of the connection line and the common line in a region of the connection line.

[CLAIM 55]

The method of claim 29, wherein the step of forming the gate line includes a step of forming a gate pad at an end of the gate line, and the step of forming the data line includes a step of forming a data pad at an end of the data line.

[CLAIM 56]

The method of claim 55, wherein the step of forming the photoresist pattern includes a step of forming second and third opening portions on the photoresist pattern, wherein the second and third opening portions expose the gate and data pad, respectively.

[CLAIM 57]

The method of claim 56, wherein the step of etching the passivation layer includes a step of removing the transparent conductive material exposed by the second and third opening portions.

[CLAIM 58]

The method of claim 57, wherein the gate pad is exposed by etching the gate insulating layer and the passivation layer in the second opening portion, and the data pad is exposed by etching the passivatino layer in the third opening portion.

[CLAIM 59]

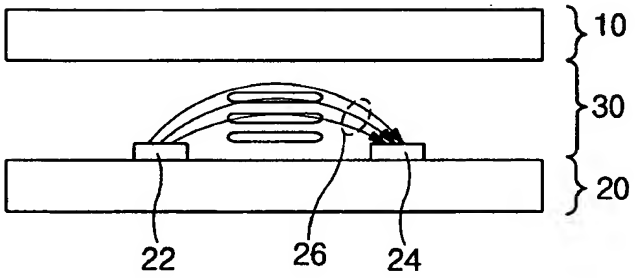
The method of claim 58, wherein the transparent conductive material remained in the second opening portion is the gate pad electrode connected to the gate pad, and the transparent conductive material remained in the third opening portion is the data pad electrode connected to the data pad.

[CLAIM 60]

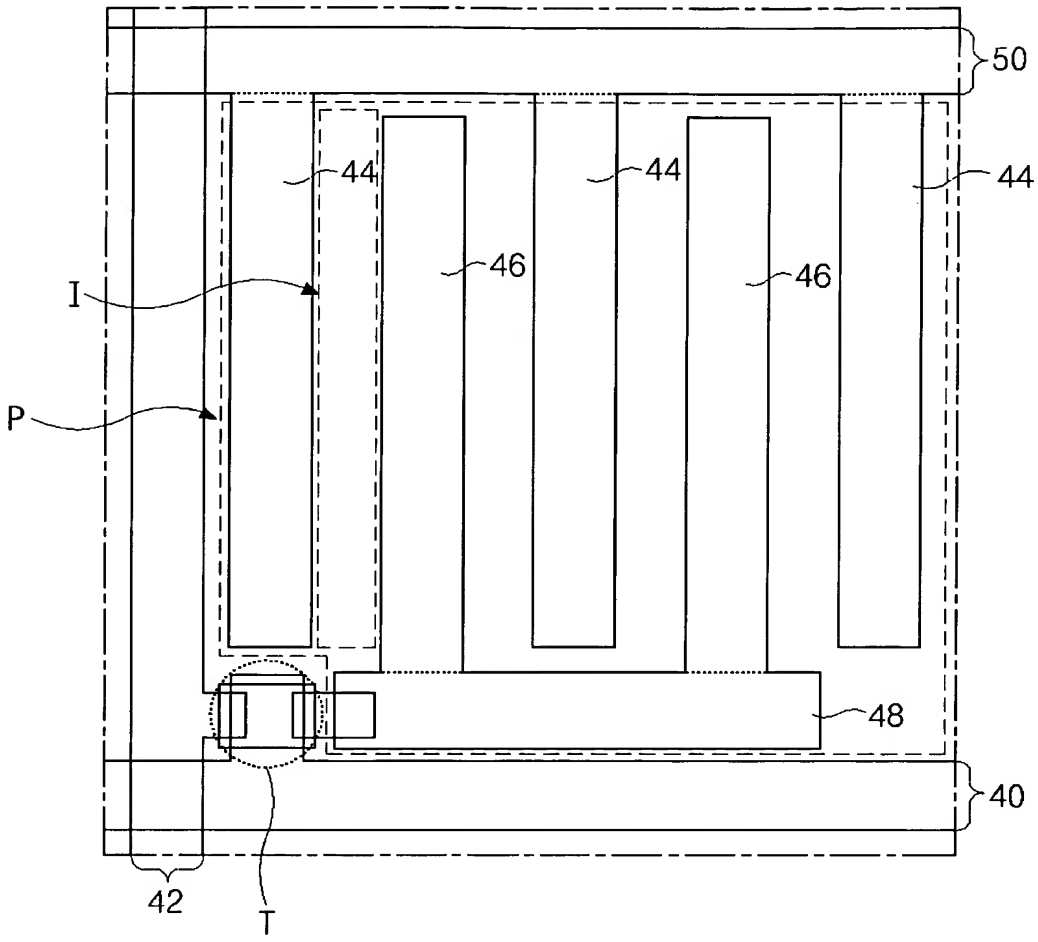
The method of claim 29, wherein the opening portion includes first, second and third sub-opening portions, wherein the first and second sub-opening portions are spaced apart from each other to be symmetrical to the common line, and the third sub-opening portion is located at a crossing portion of the connection and common lines in the connection line, wherein the pixel electrode includes first, second and third pixel electrode patterns corresponding to the first, second and third sub-opening portions.

[DRAWINGS]

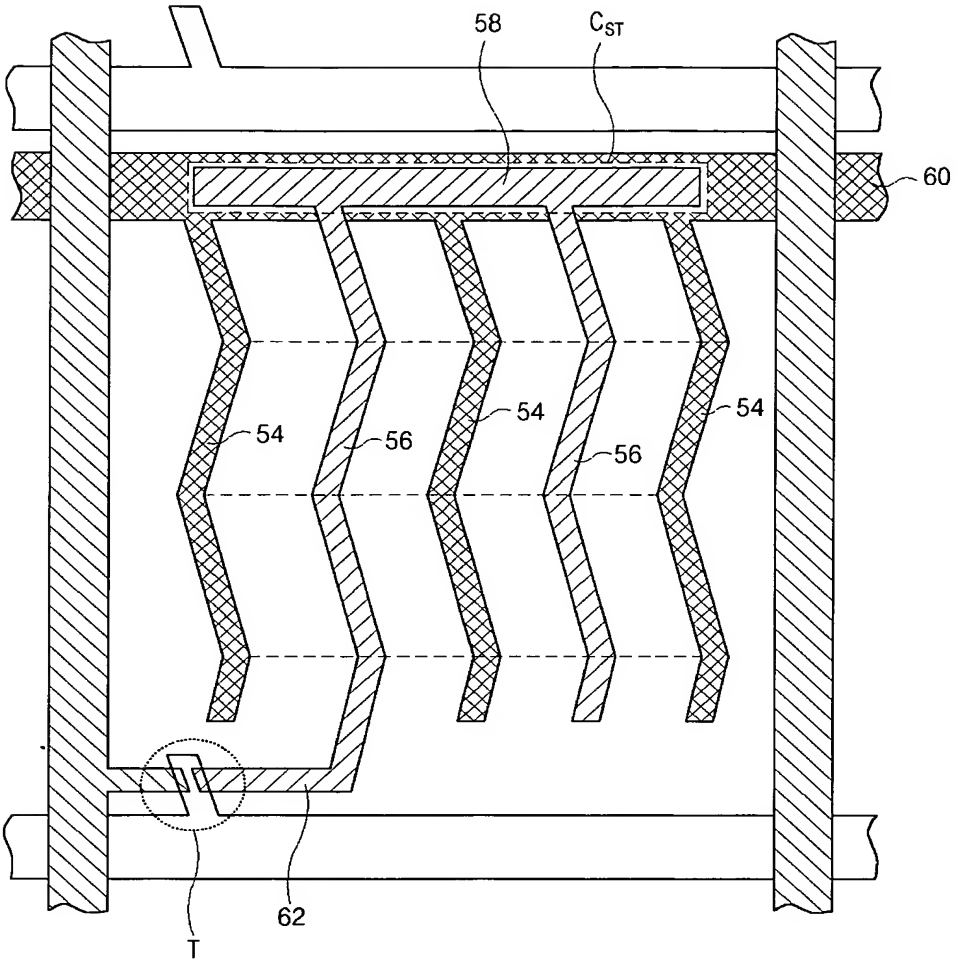
【FIG. 1】



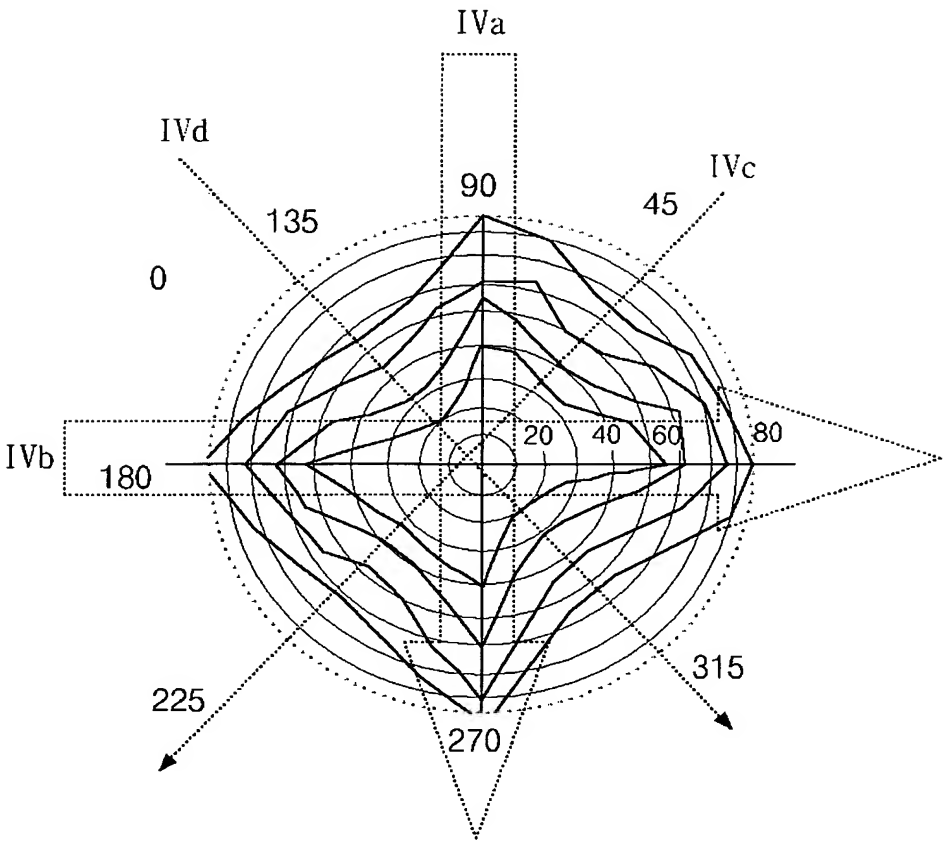
【FIG. 2】



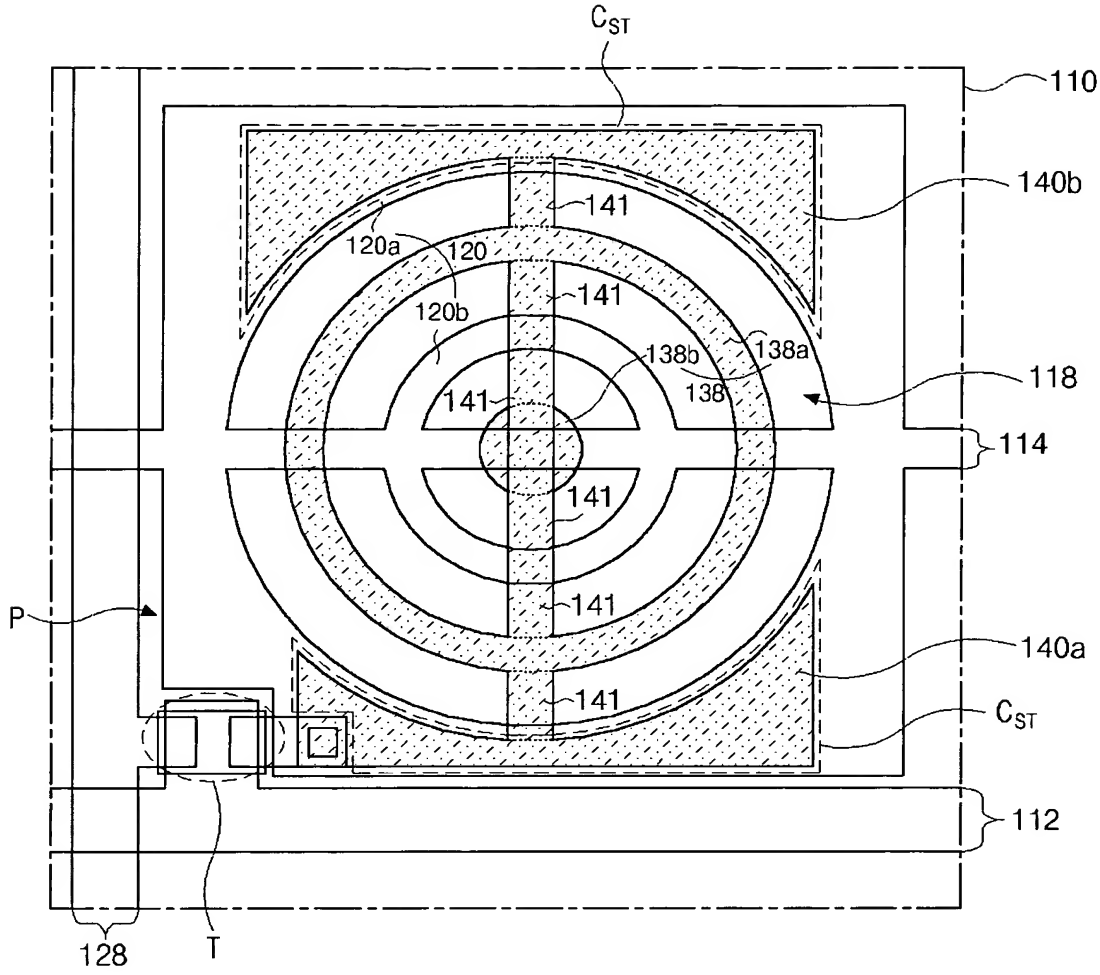
【FIG. 3】



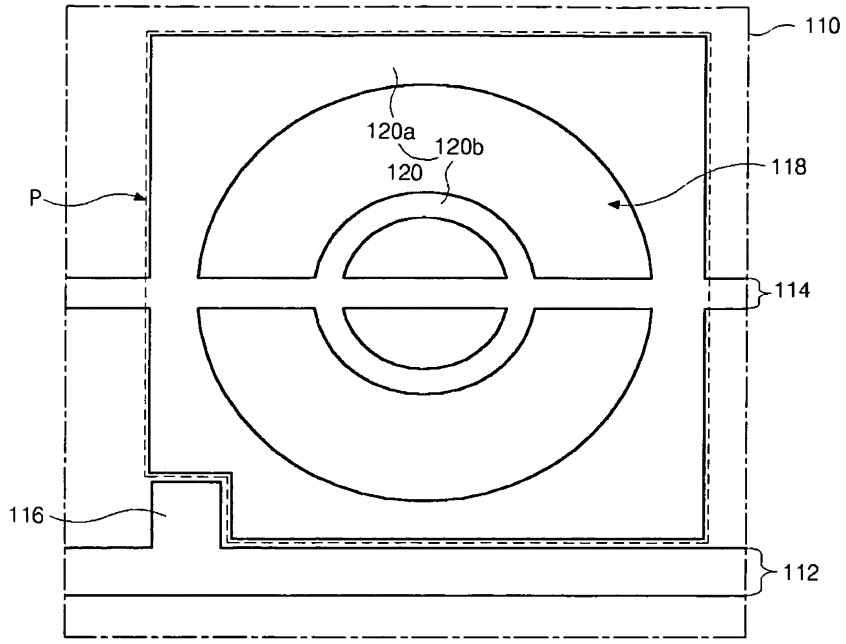
【FIG. 4】



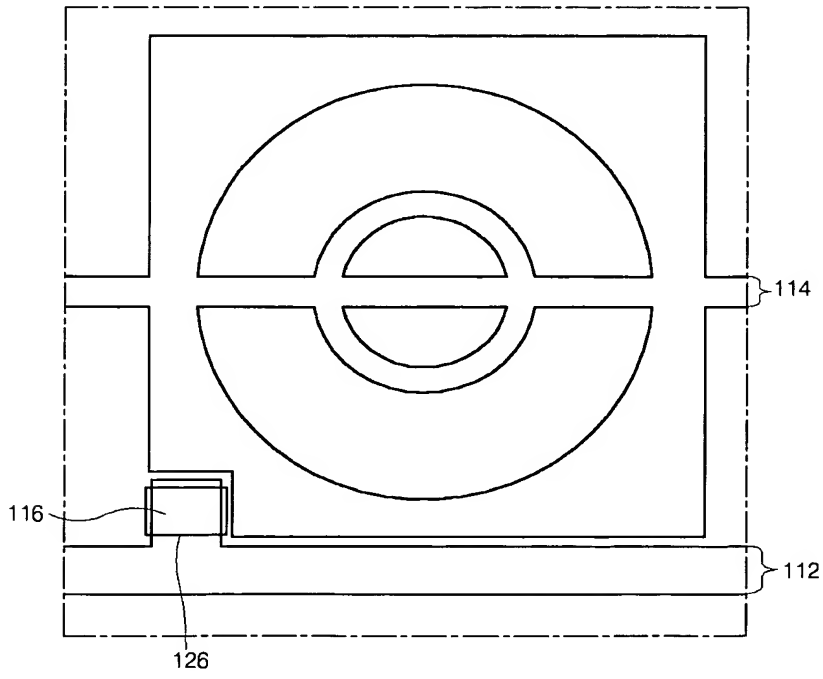
【FIG. 5】


C_{ST}
110
140b
141
120a
120
141
120b
138b
138a
118
141
138
114
141
P
141
140a
141
C_{ST}
112
128
T

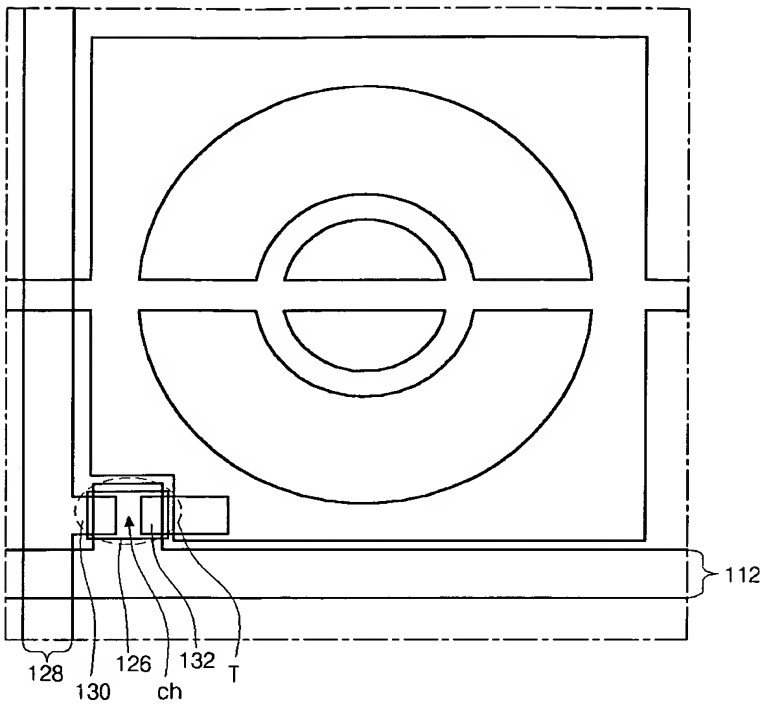
【FIG. 6A】



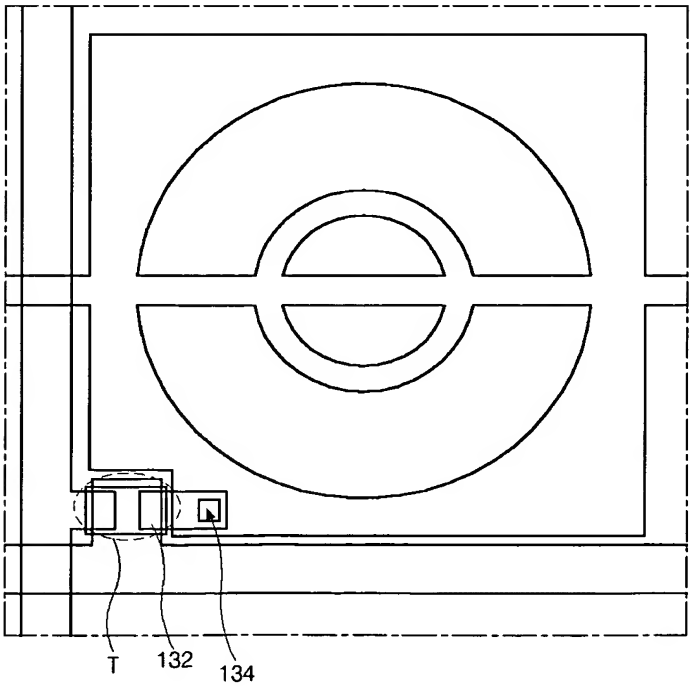
【FIG. 6B】



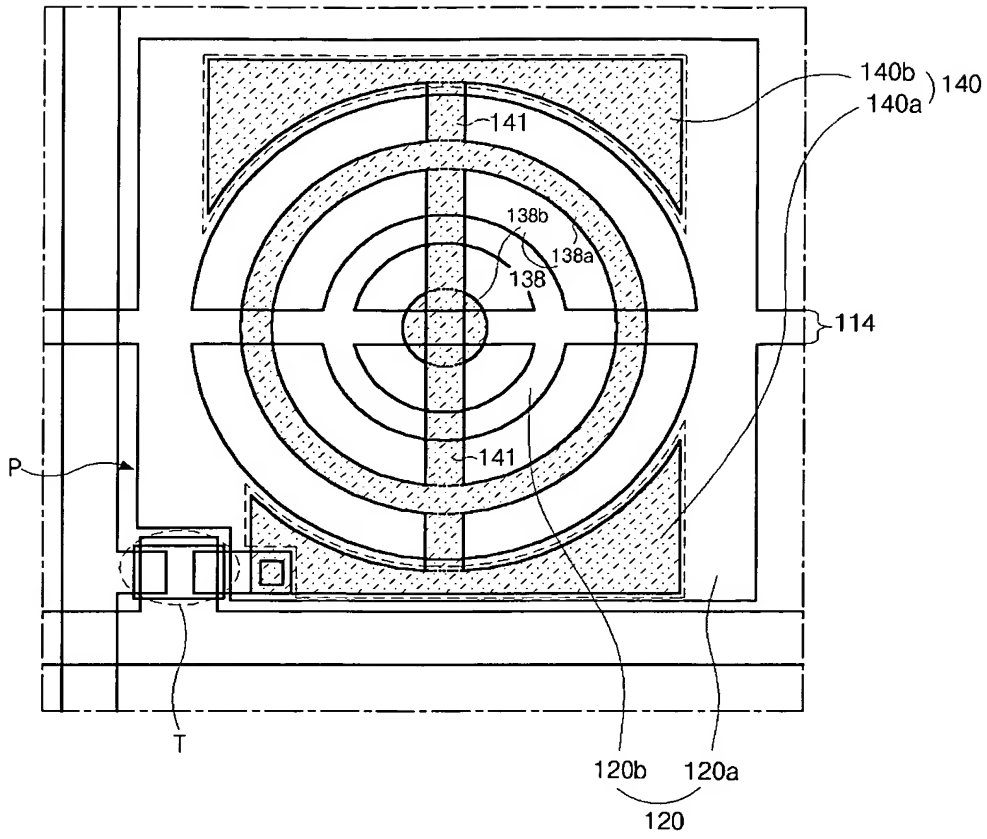
【FIG. 6C】



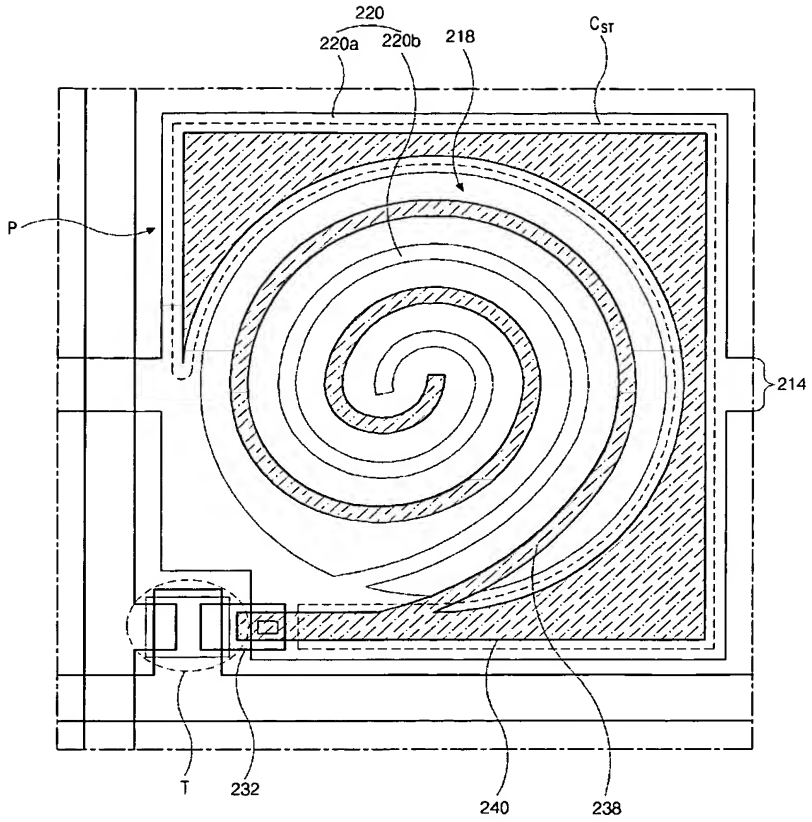
【FIG. 6D】



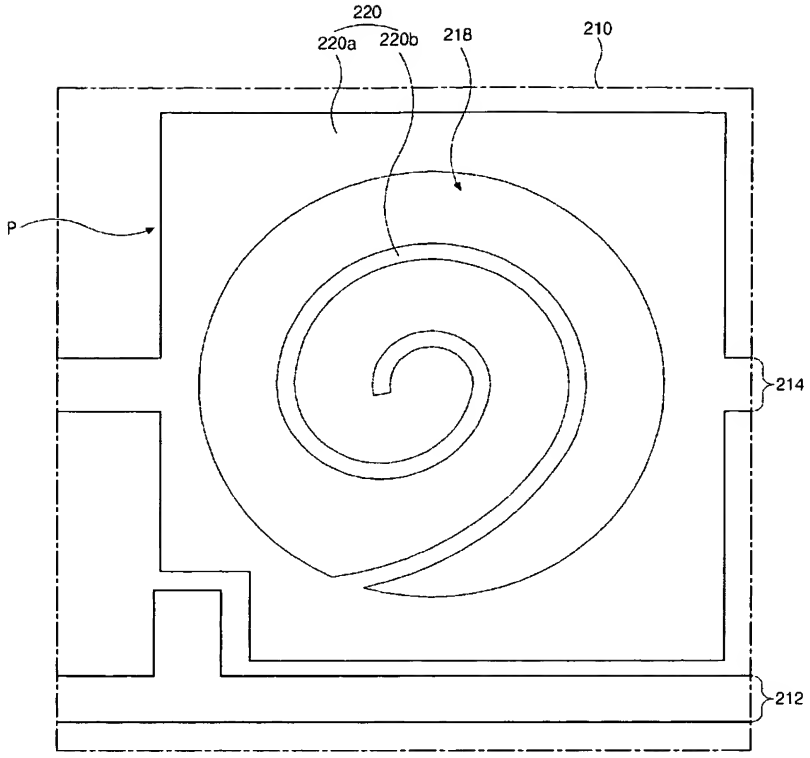
【FIG. 6E】



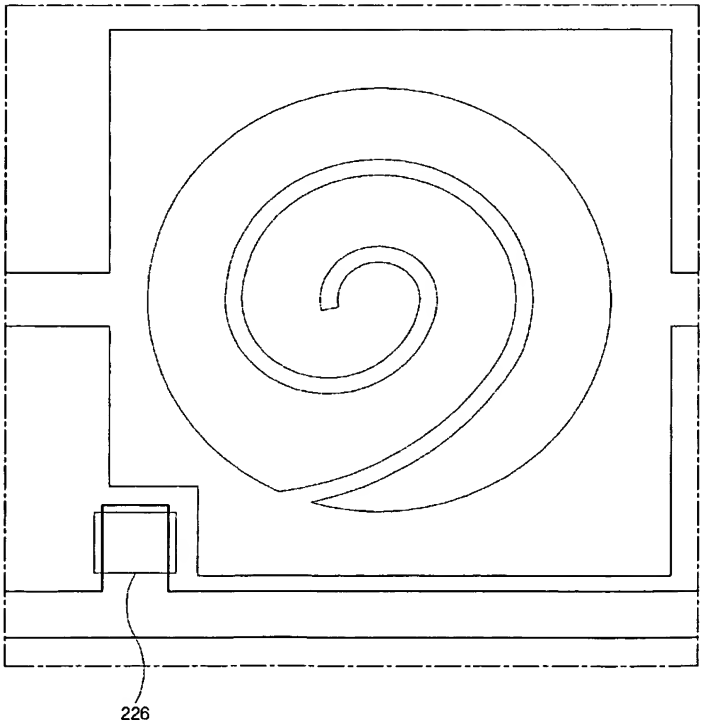
【FIG. 7】



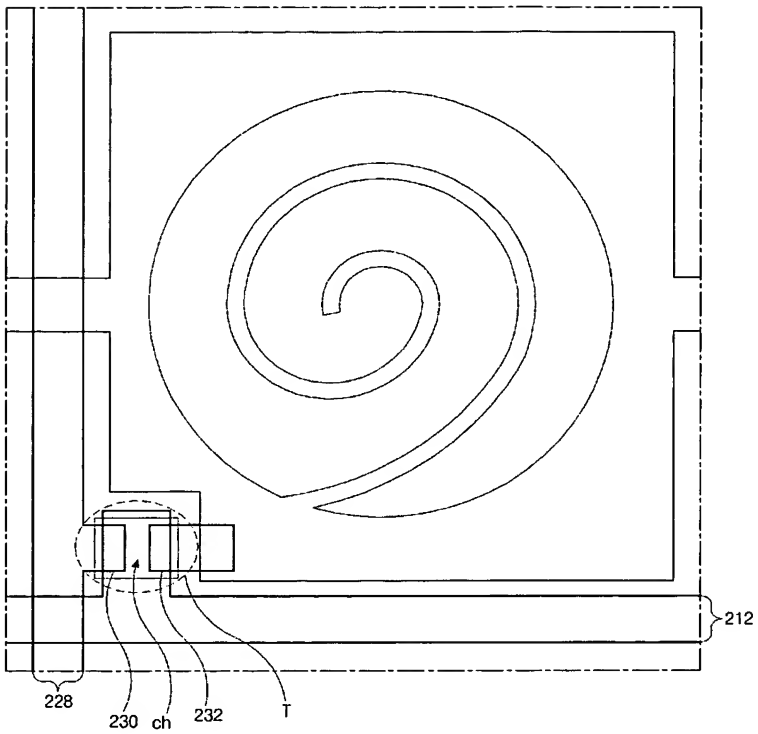
【FIG. 8A】



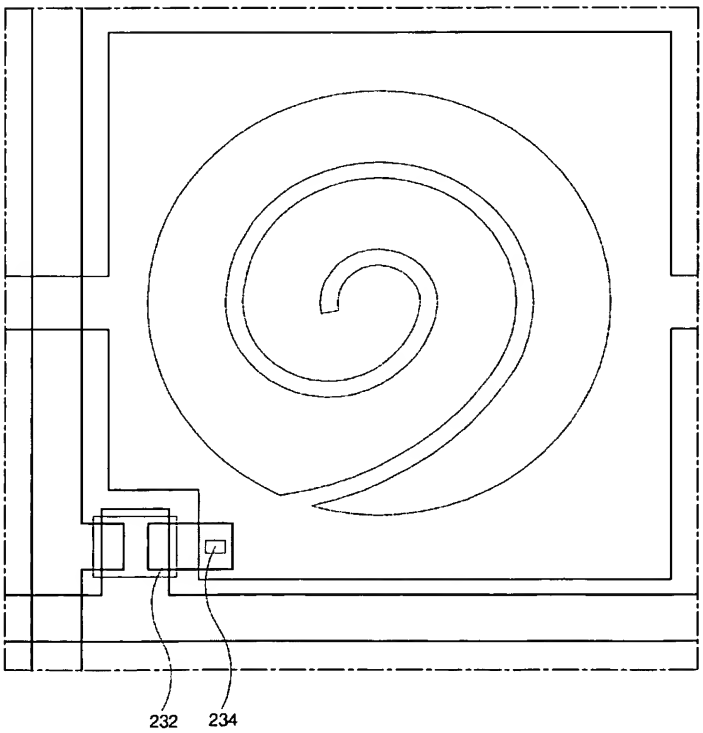
【FIG. 8B】



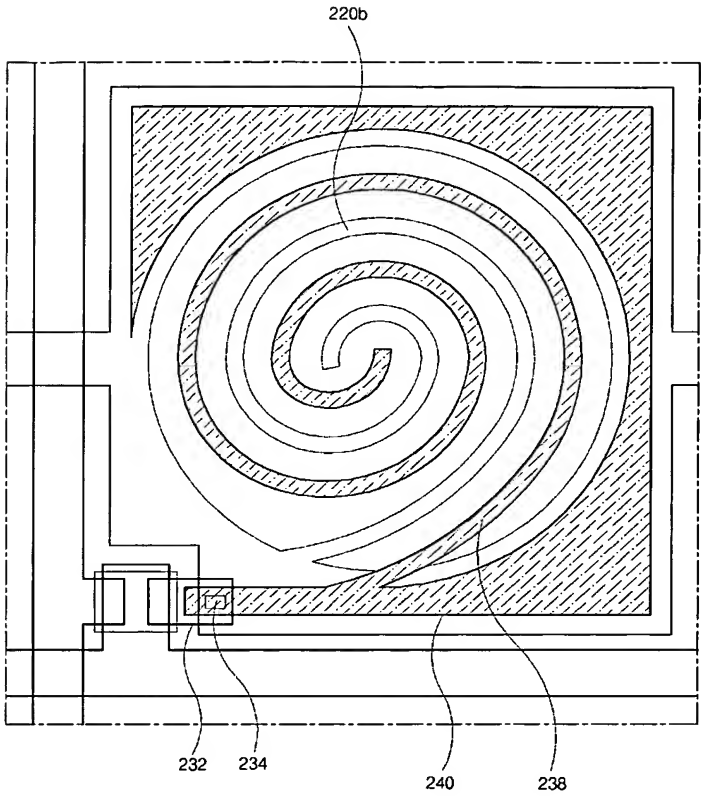
【FIG. 8C】



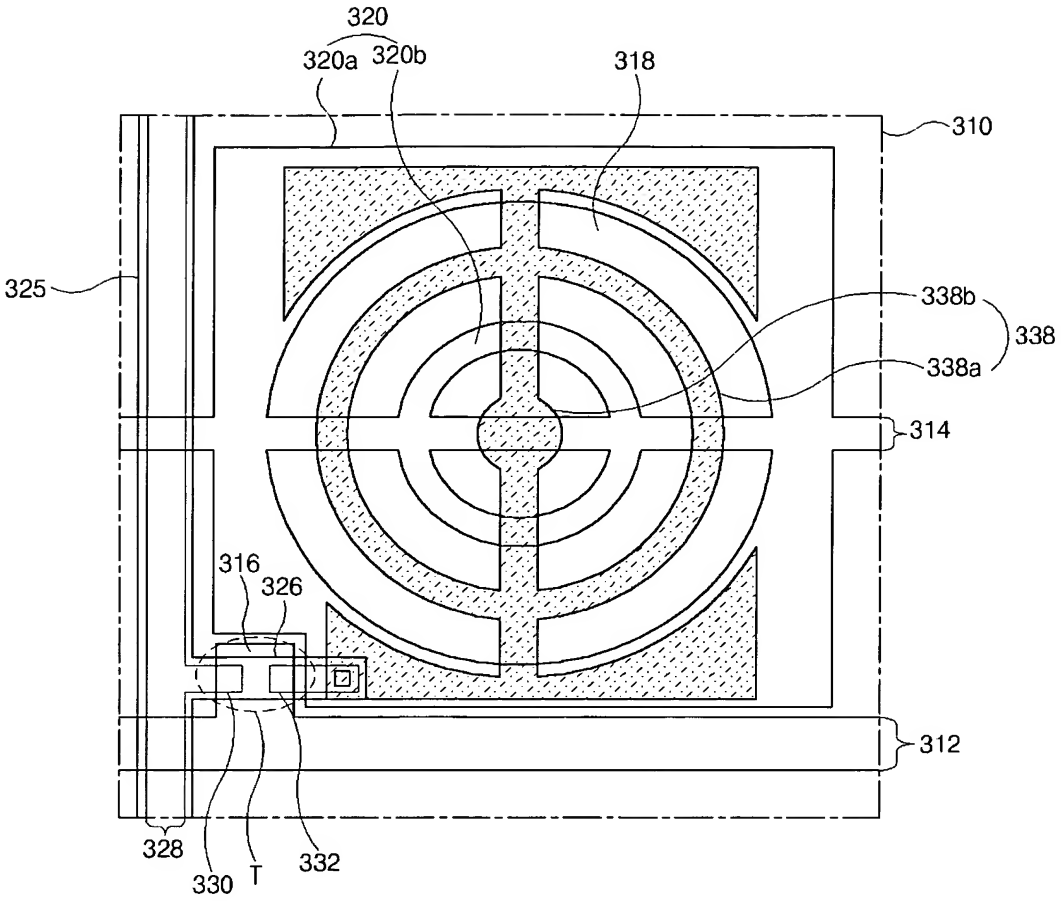
【FIG. 8D】



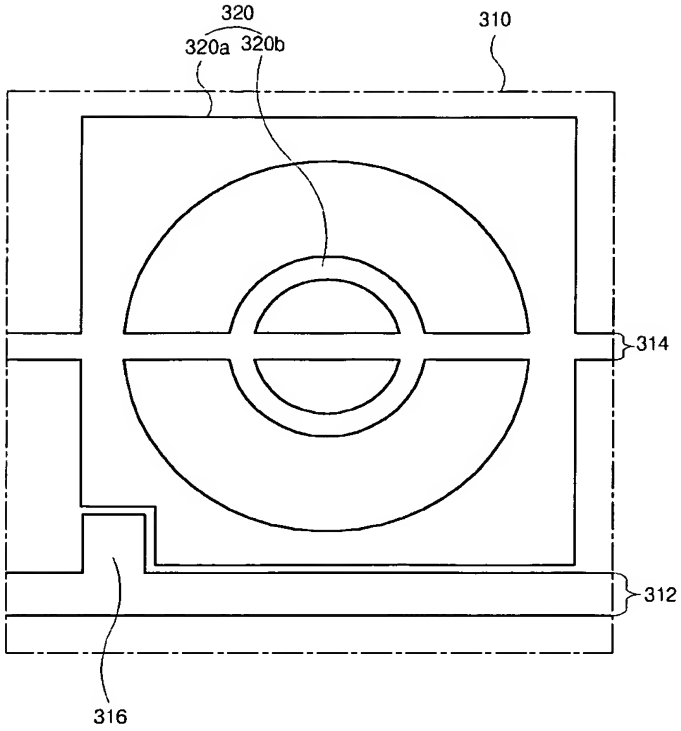
【FIG. 8E】



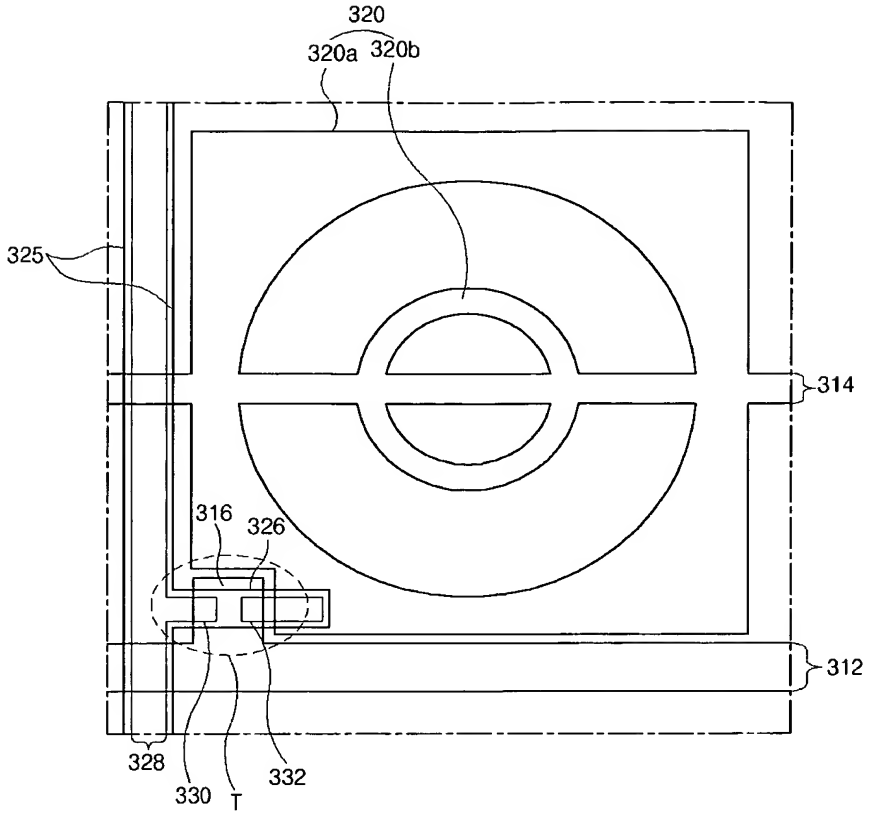
【FIG. 9】


320
320a
320b
318
310
325
338b
338
338a
314
316
326
312
328
330
T
332

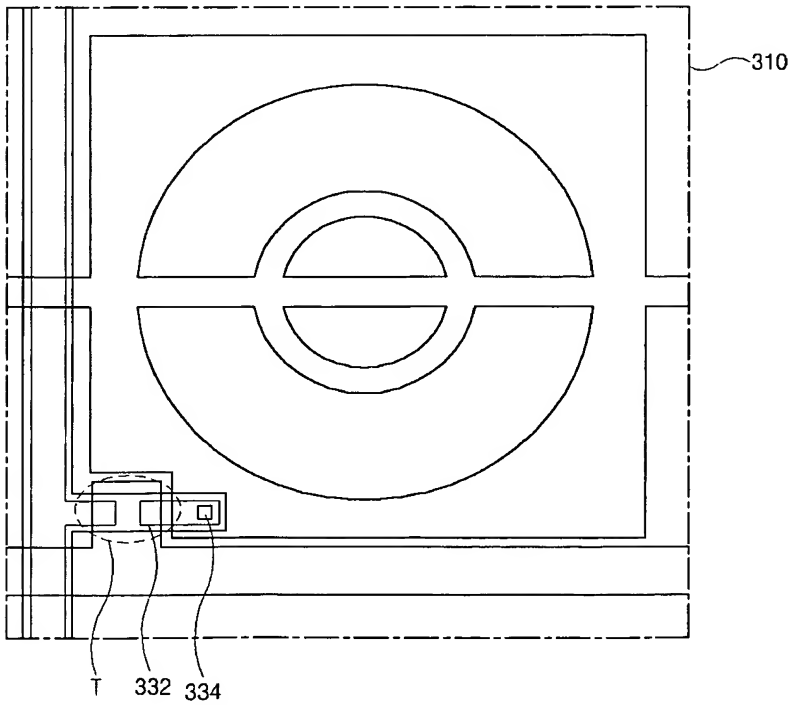
【FIG. 10A】



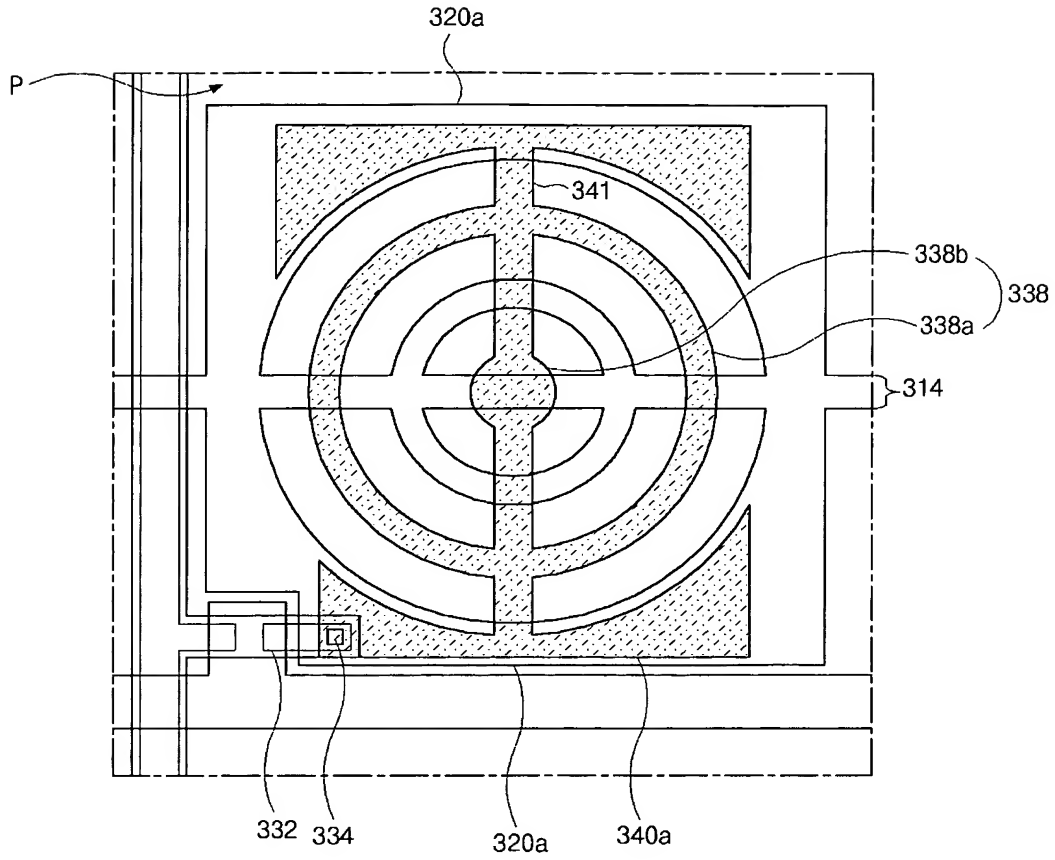
【FIG. 10B】



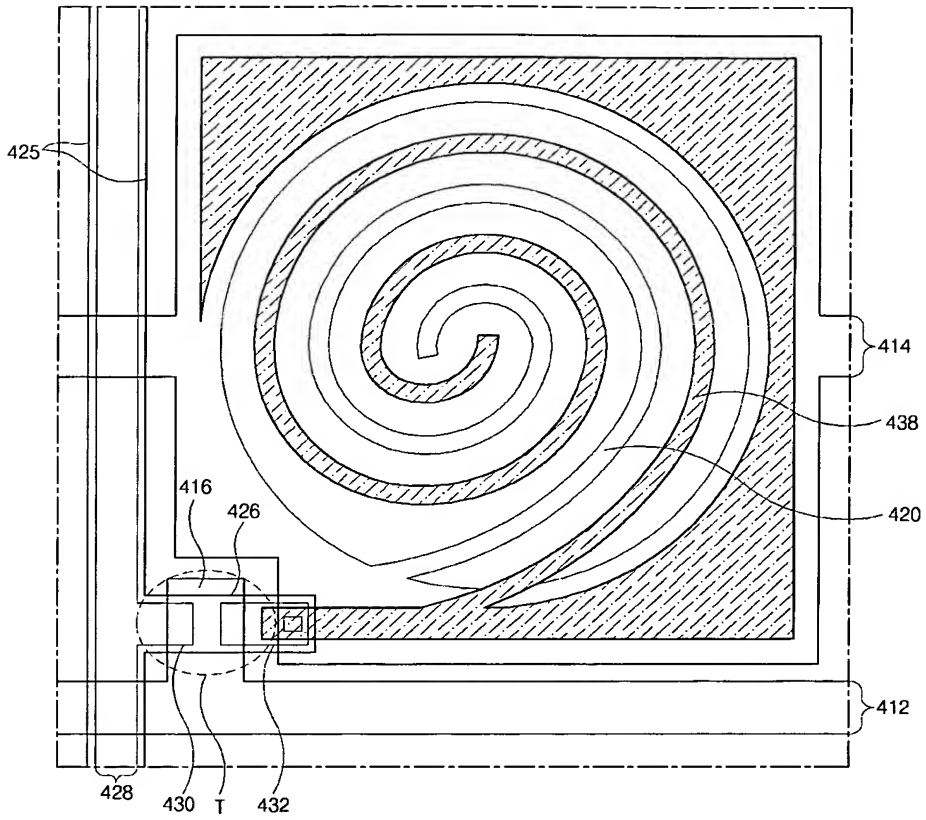
【FIG. 10C】



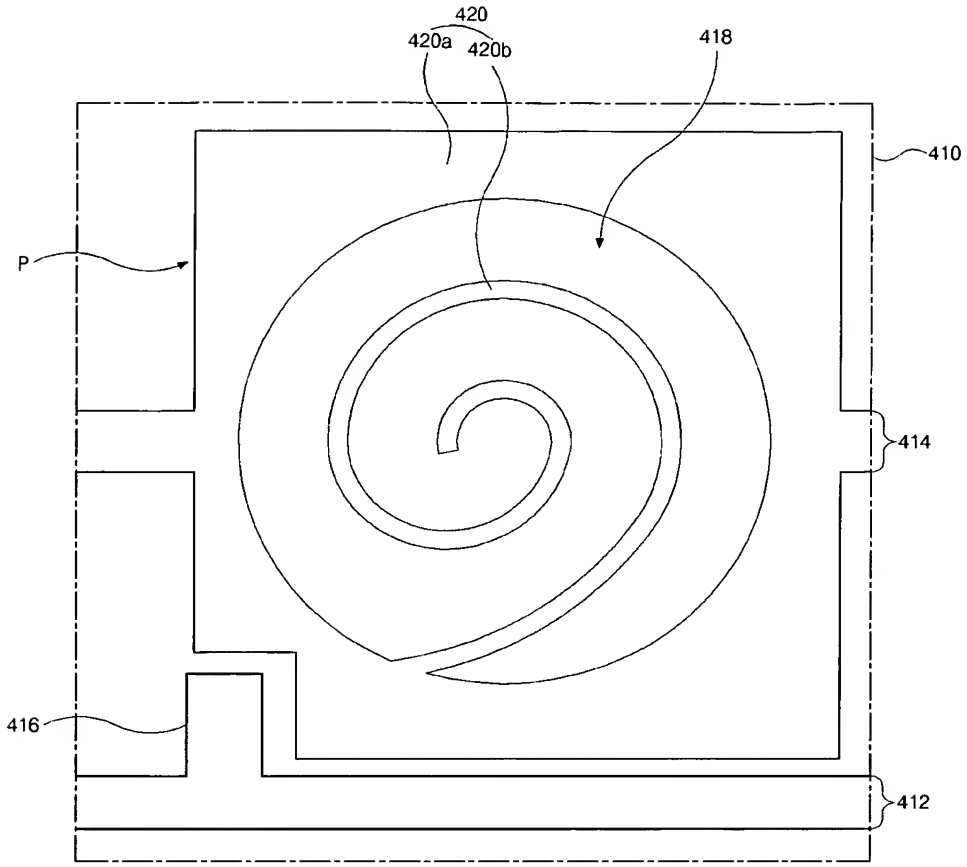
【FIG. 10D】



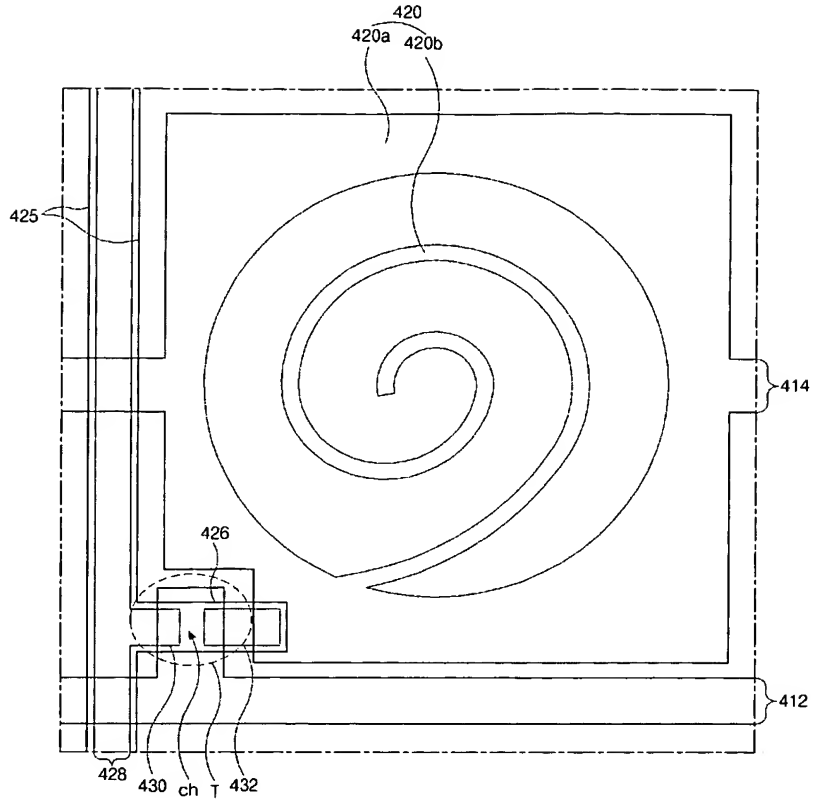
【FIG. 11】



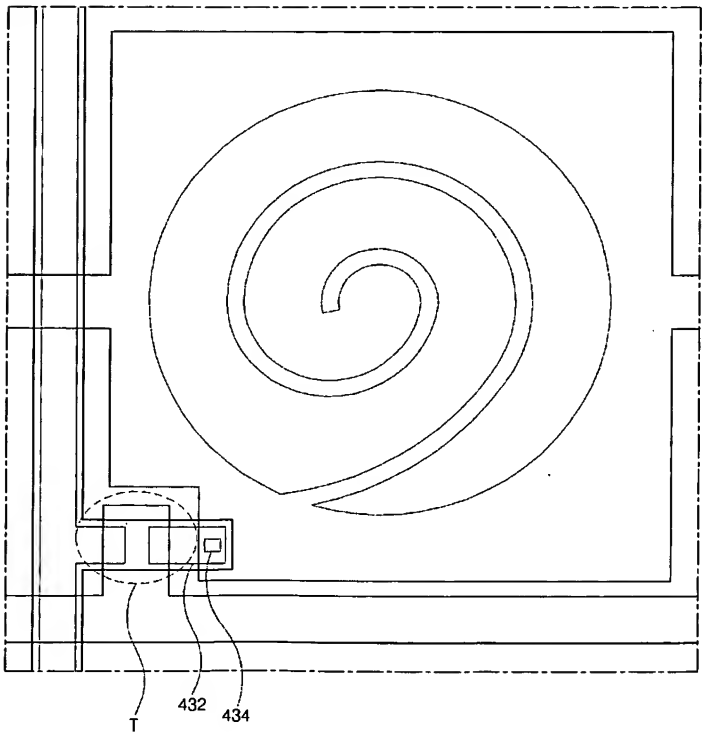
【FIG. 12A】



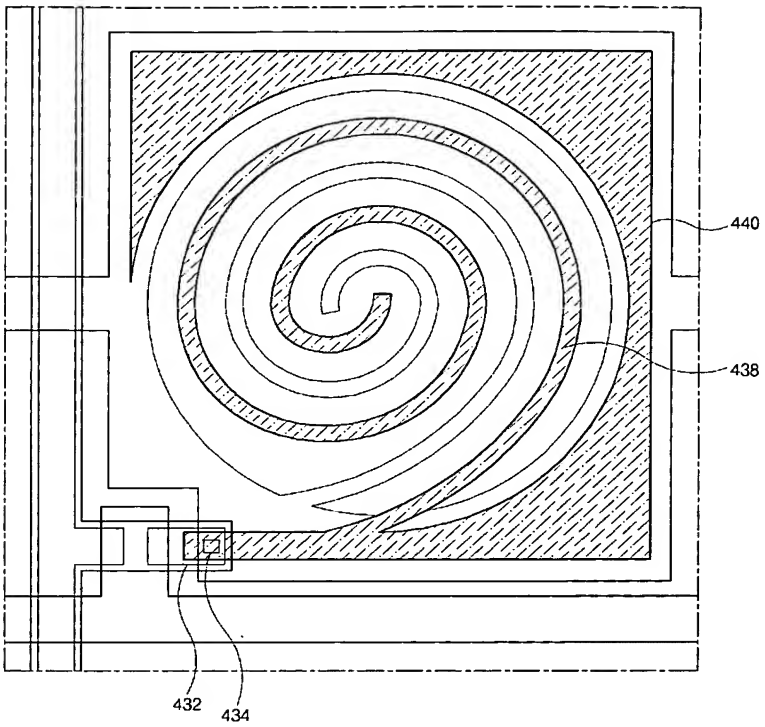
【FIG. 12B】



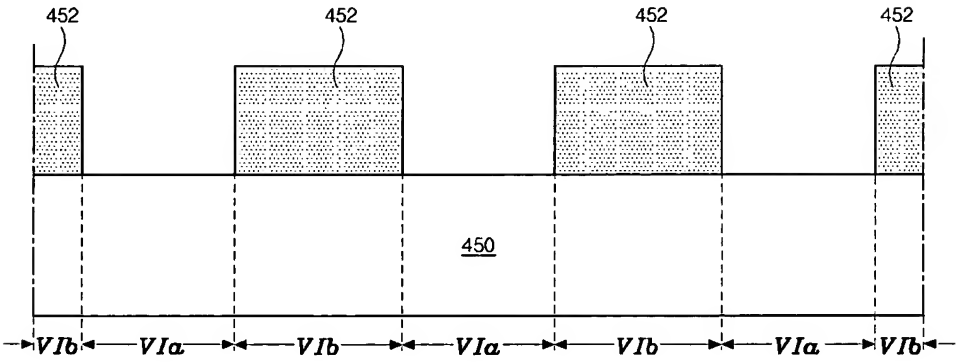
【FIG. 12C】



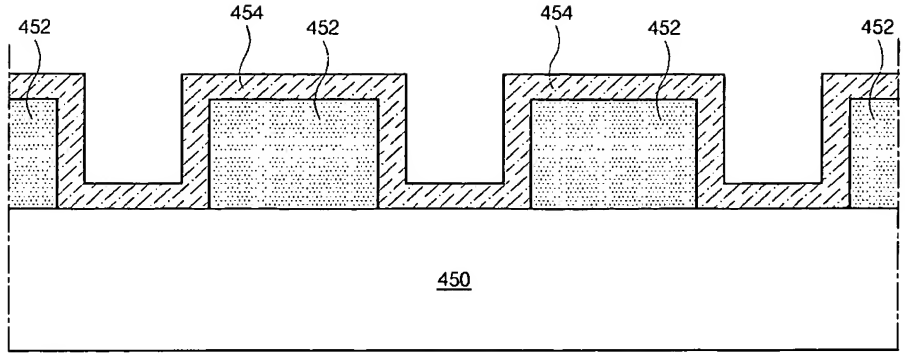
【FIG. 12D】



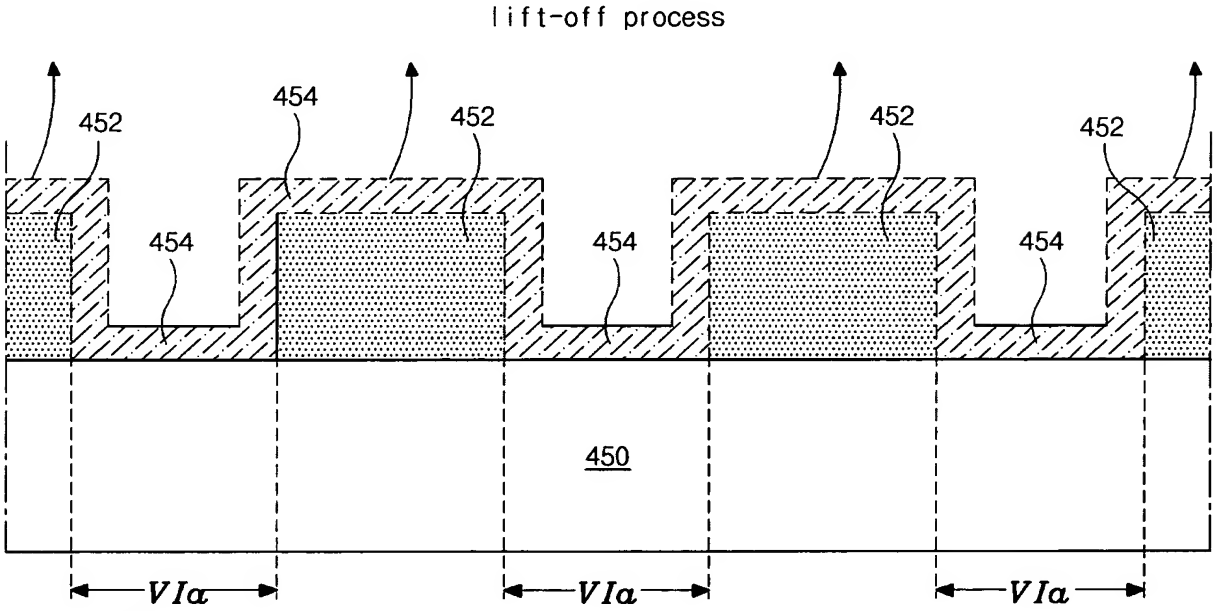
【FIG. 13A】



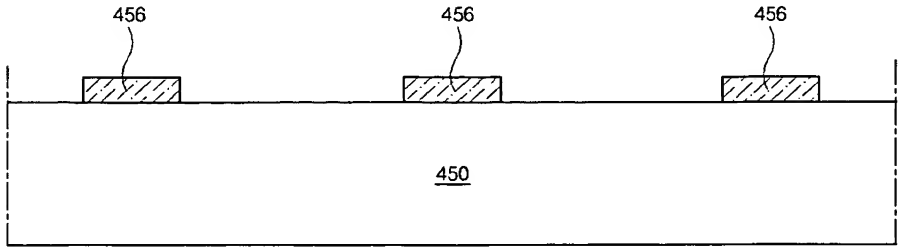
【FIG. 13B】



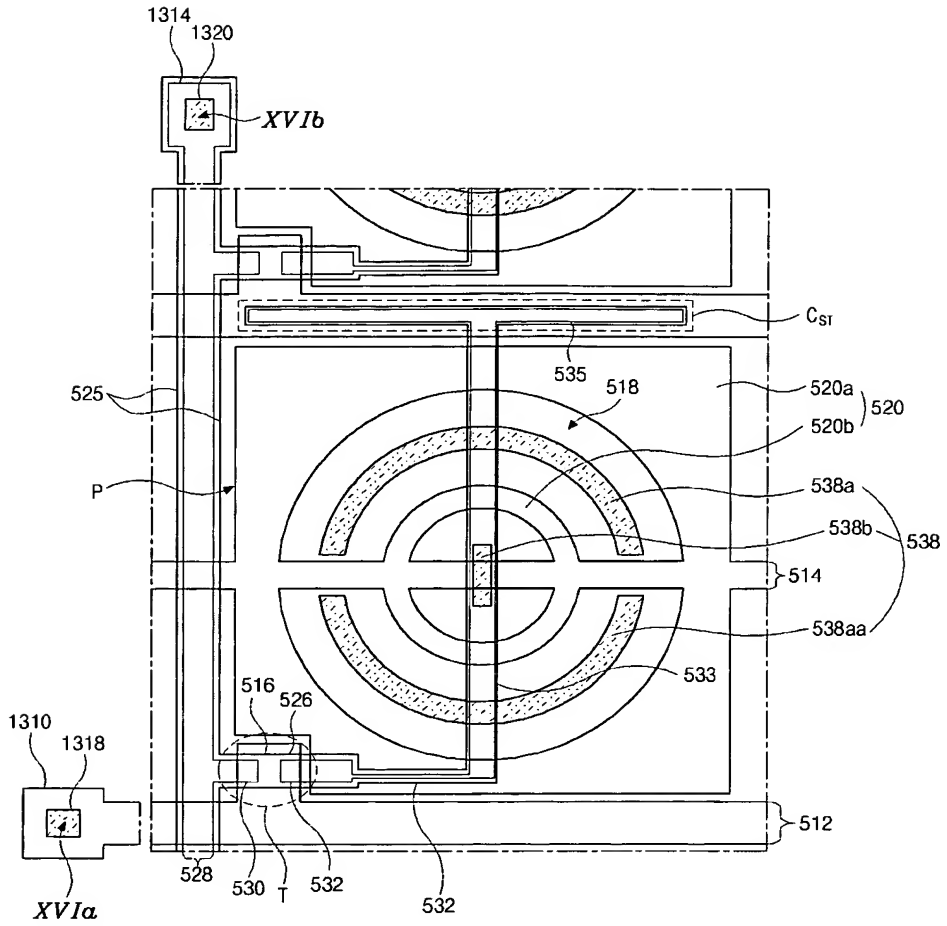
【FIG. 13C】



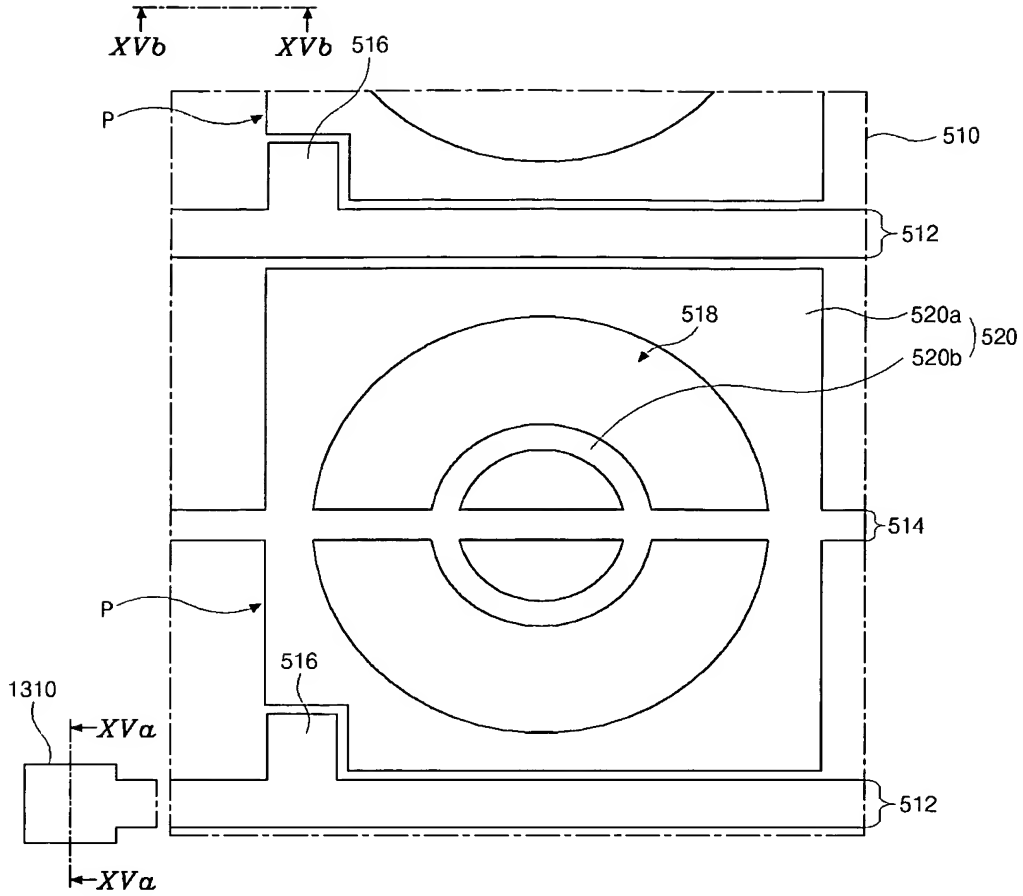
【FIG. 13D】



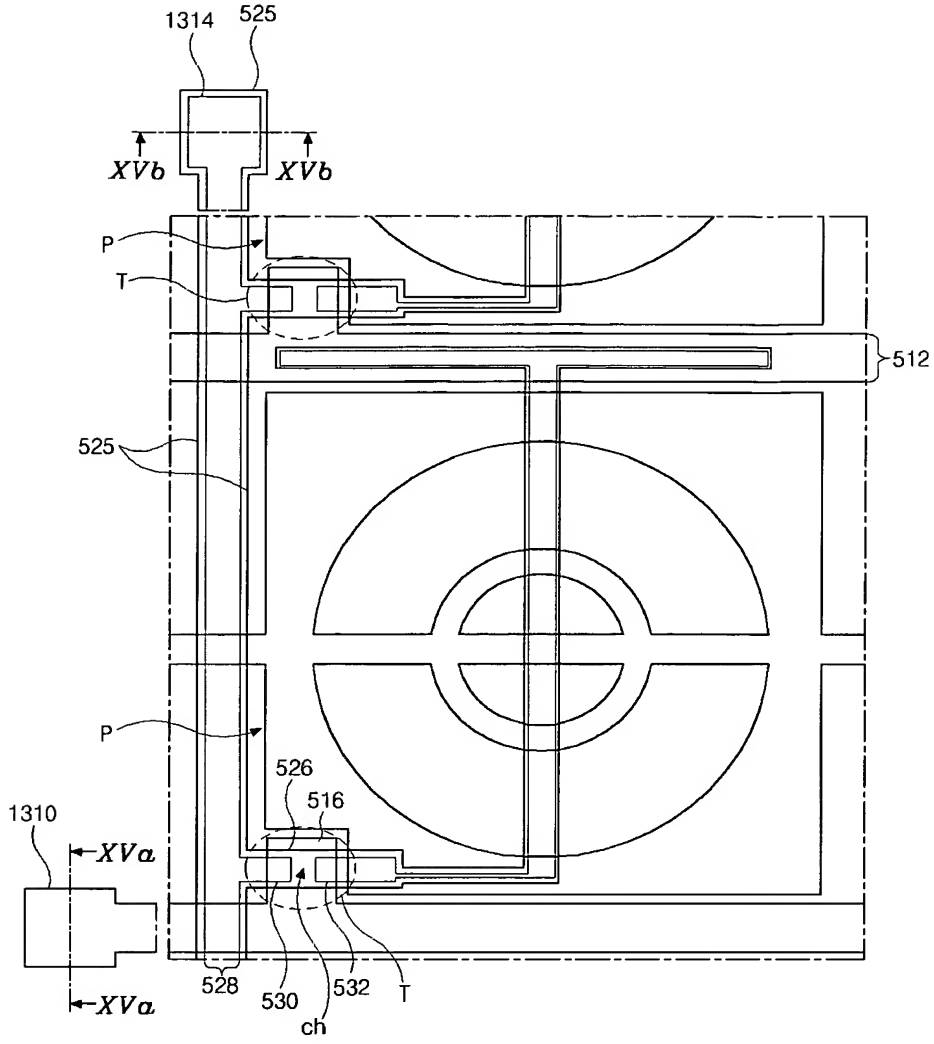
【FIG. 14】


1314
1320
XVIb
C_{ST}
535
518
520a
520
520b
525
P
538a
538b
538
514
538aa
533
516
526
1310
1318
512
528
530
T
532
532
XVIa

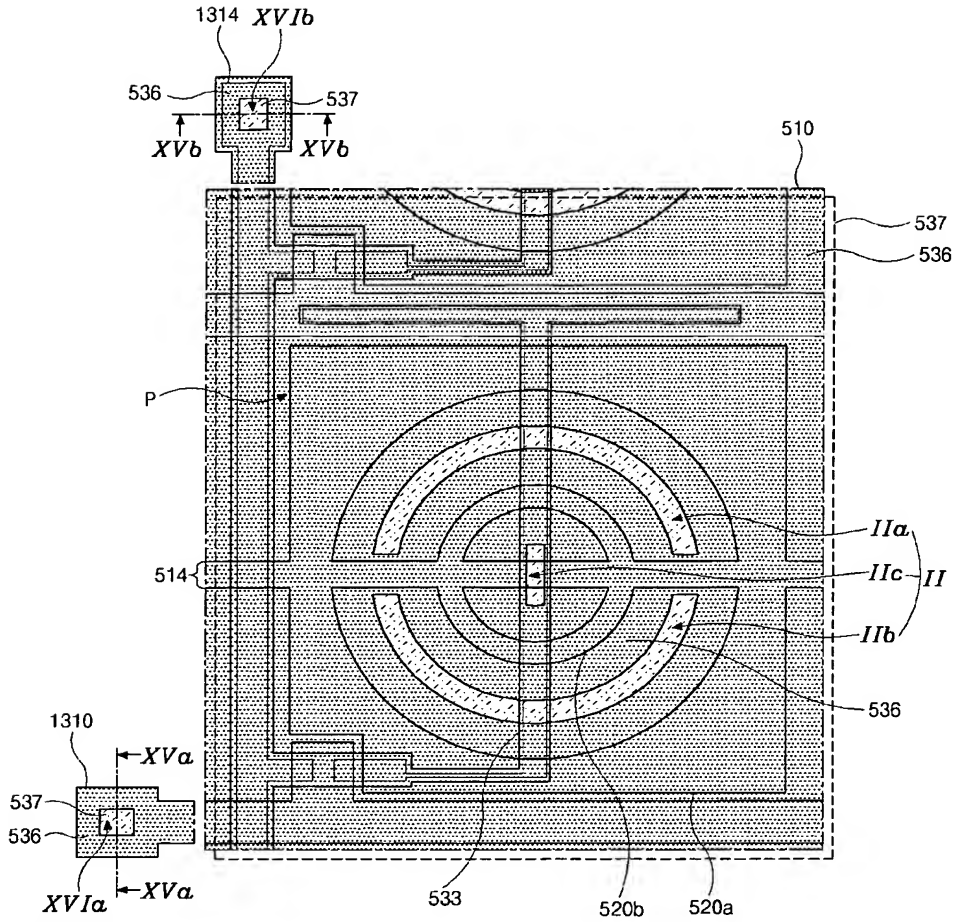
【FIG. 15A】


XVb
XVb
516
P
510
512
518
520a
520b
520
514
P
516
1310
XVa
XVa
512

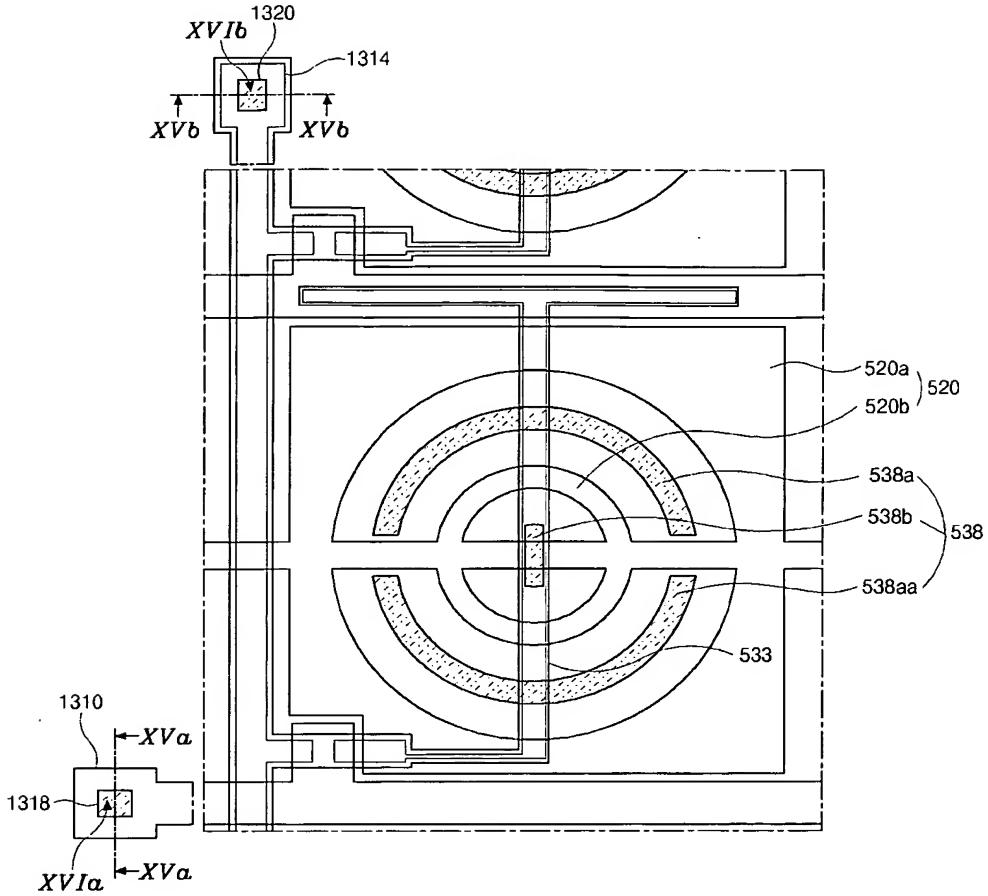
【FIG. 15B】


1314
525
XVb
XVb
P
T
512
525
P
526
516
1310
XVa
XVa
528
530
532
T
ch

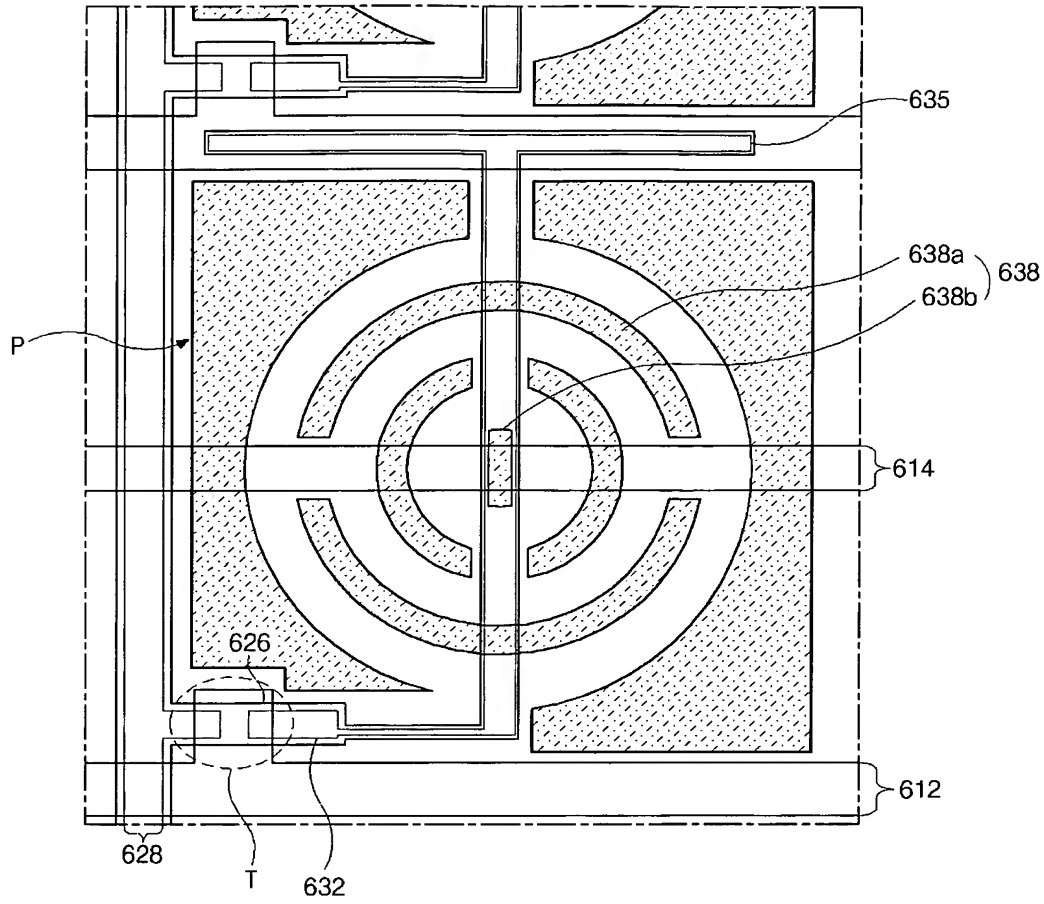
【FIG. 15C】


1314
XVIb
536
537
XVb
XVb
510
537
536
P
514
IIa
IIc
II
IIb
536
1310
XVa
537
536
XVIa
XVa
533
520b
520a

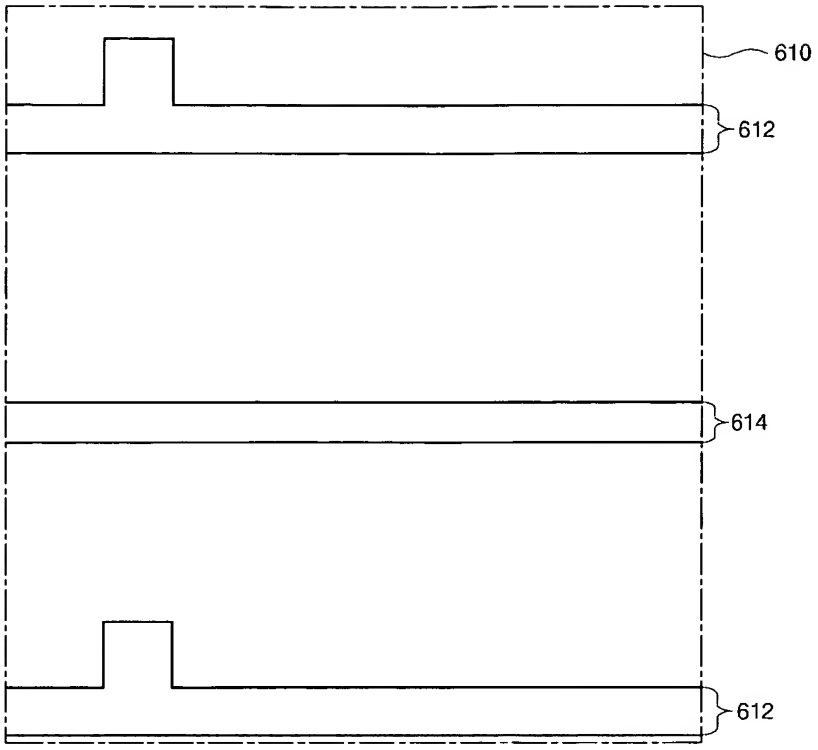
【FIG. 15D】


1320
XVIb
1314
XVb
XVb
520a
520
520b
538a
538b
538
538aa
533
1310
XVa
1318
XVIa
XVa

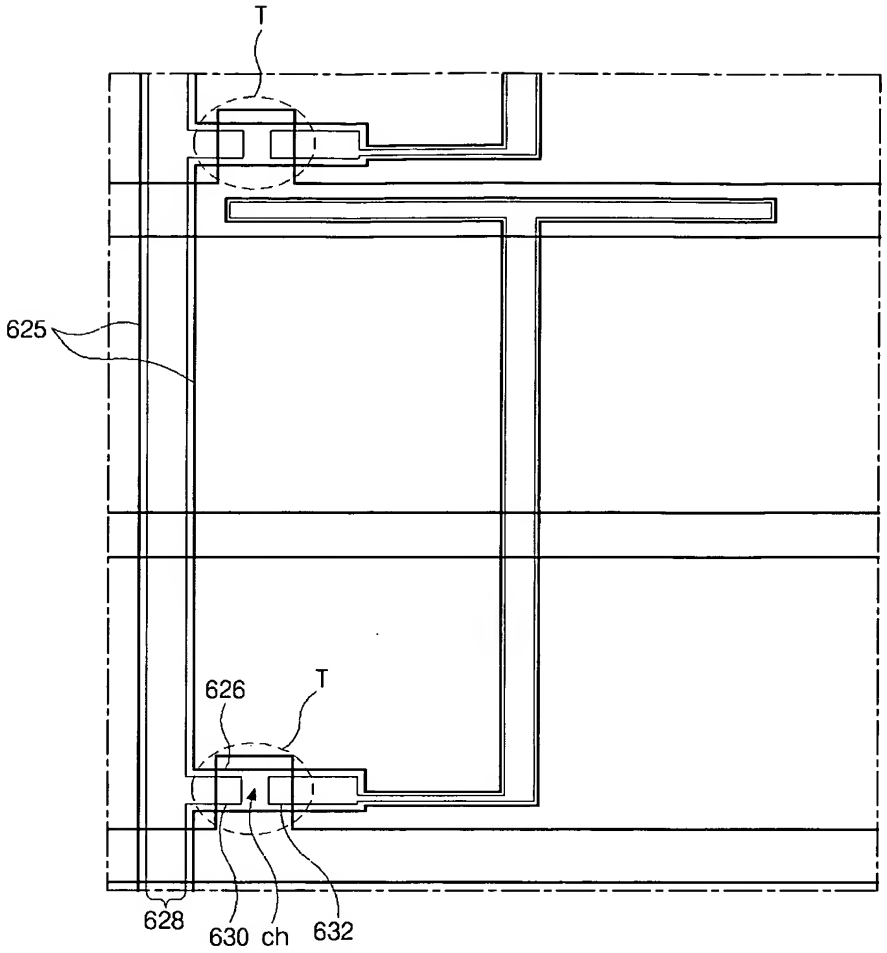
【FIG. 16】



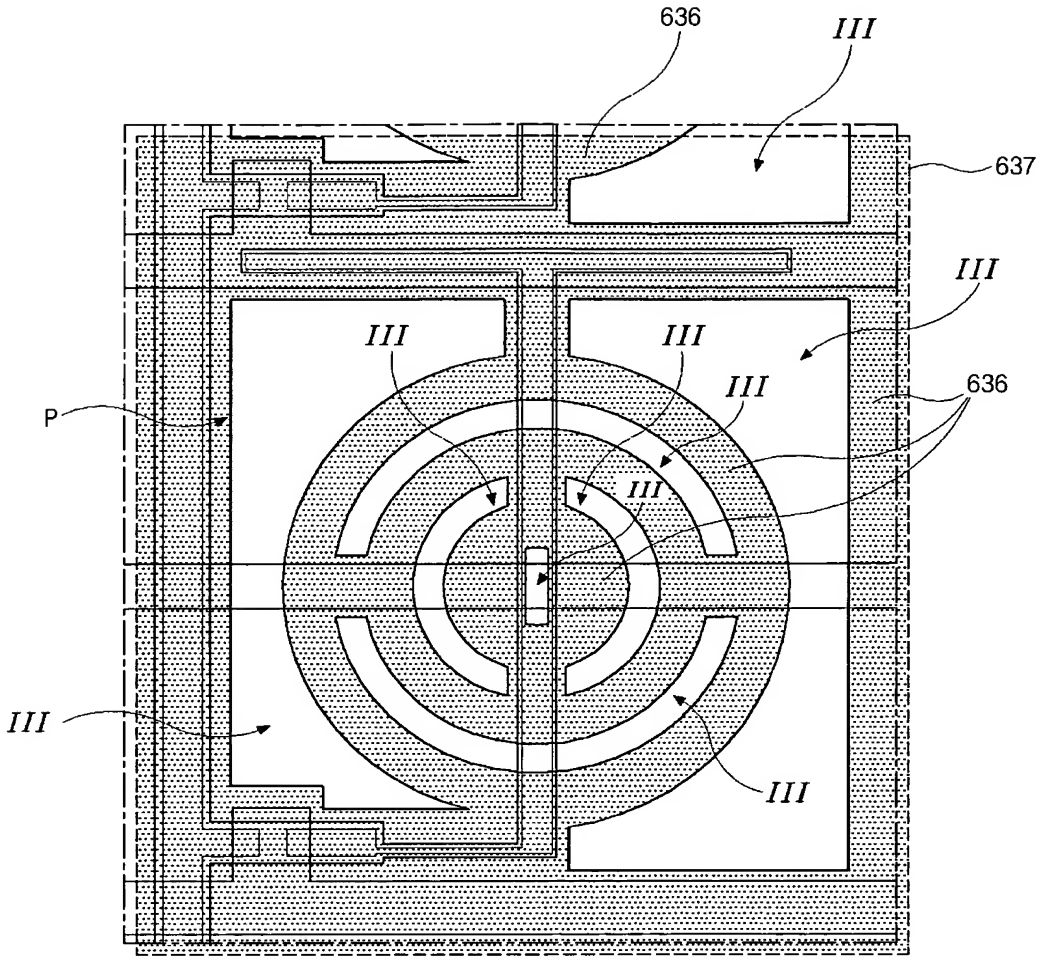
【FIG. 17A】



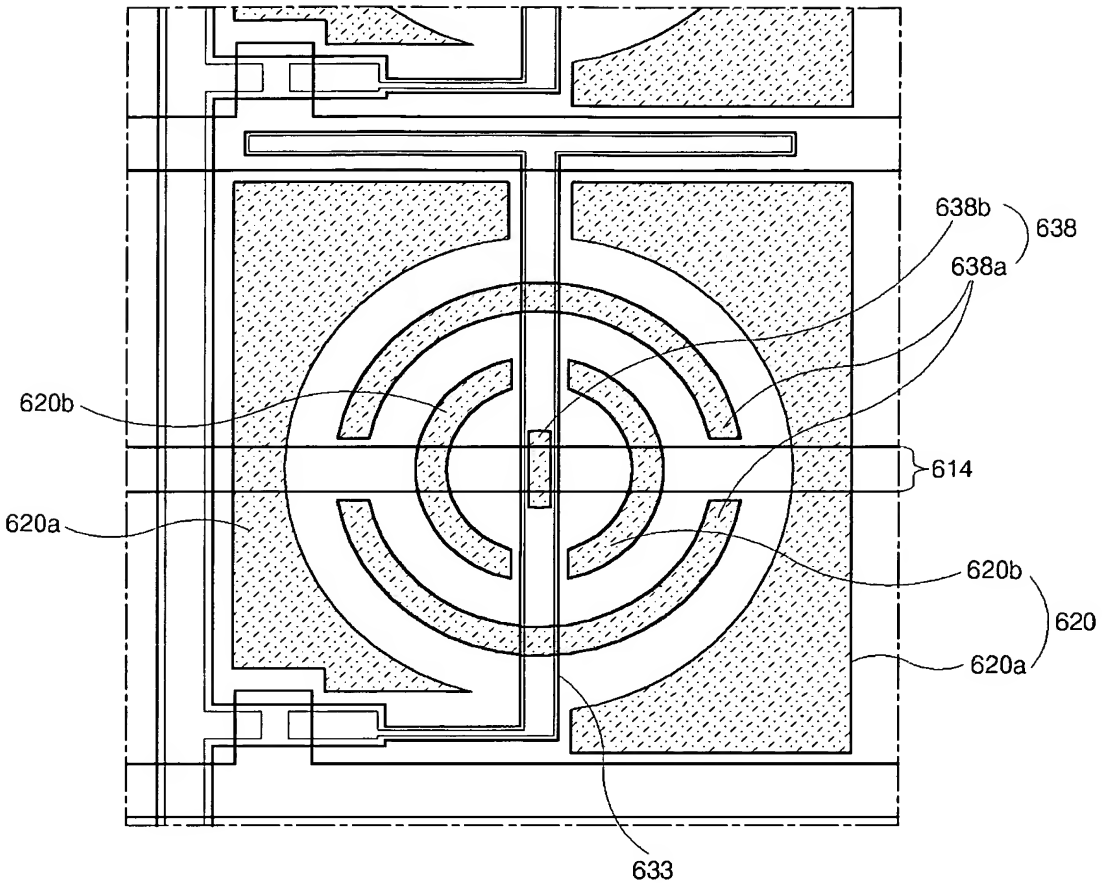
【FIG. 17B】



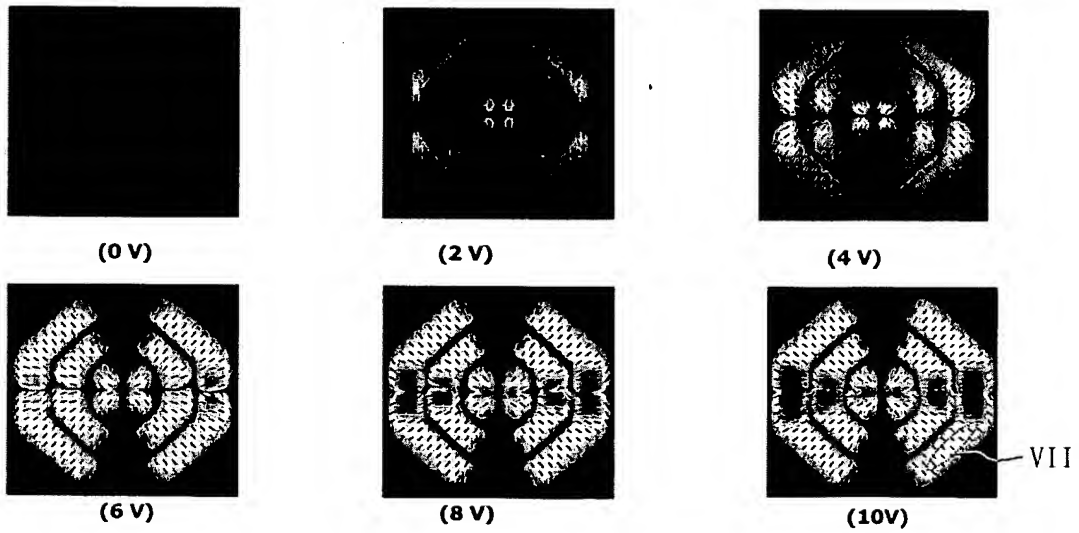
【FIG. 17C】



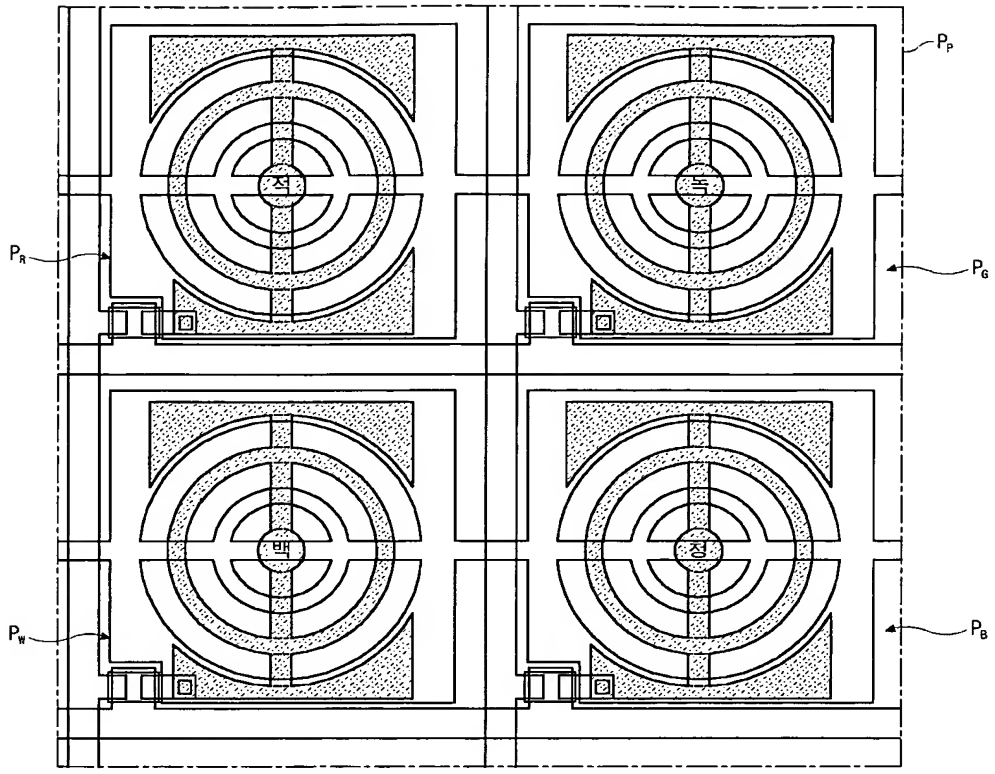
【FIG. 17D】


638b
638
638a
620b
614
620a
620b
620
620a
633

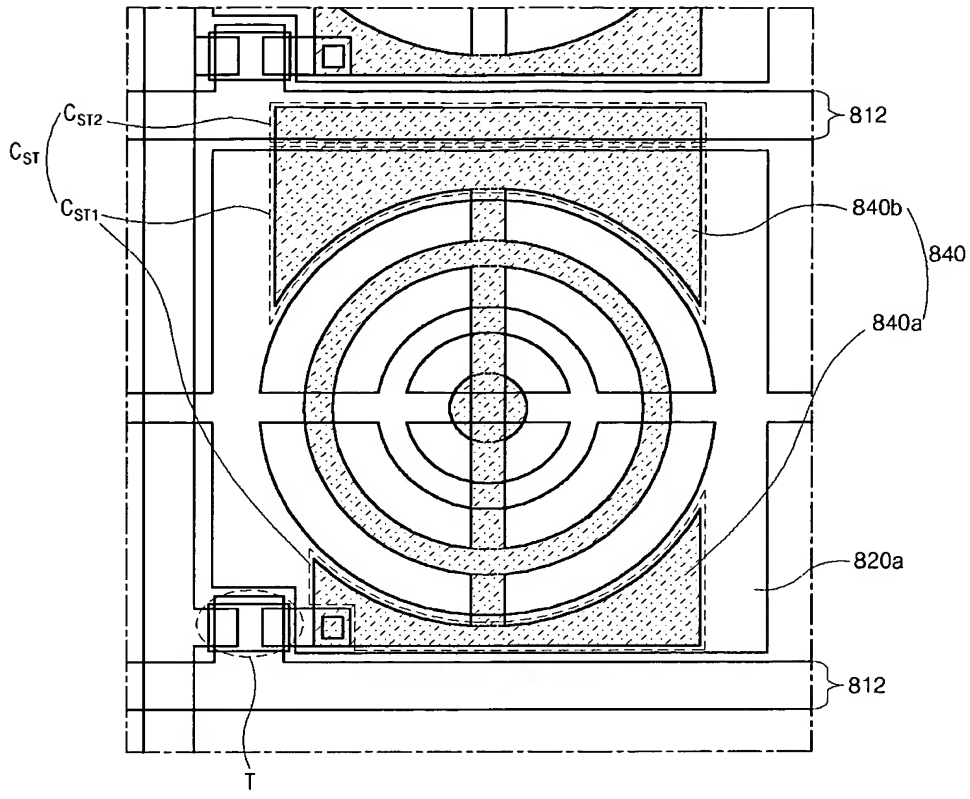
【FIG. 18】


(0 V)
(2 V)
(4 V)
(6 V)
(8 V)
(10V)
VII

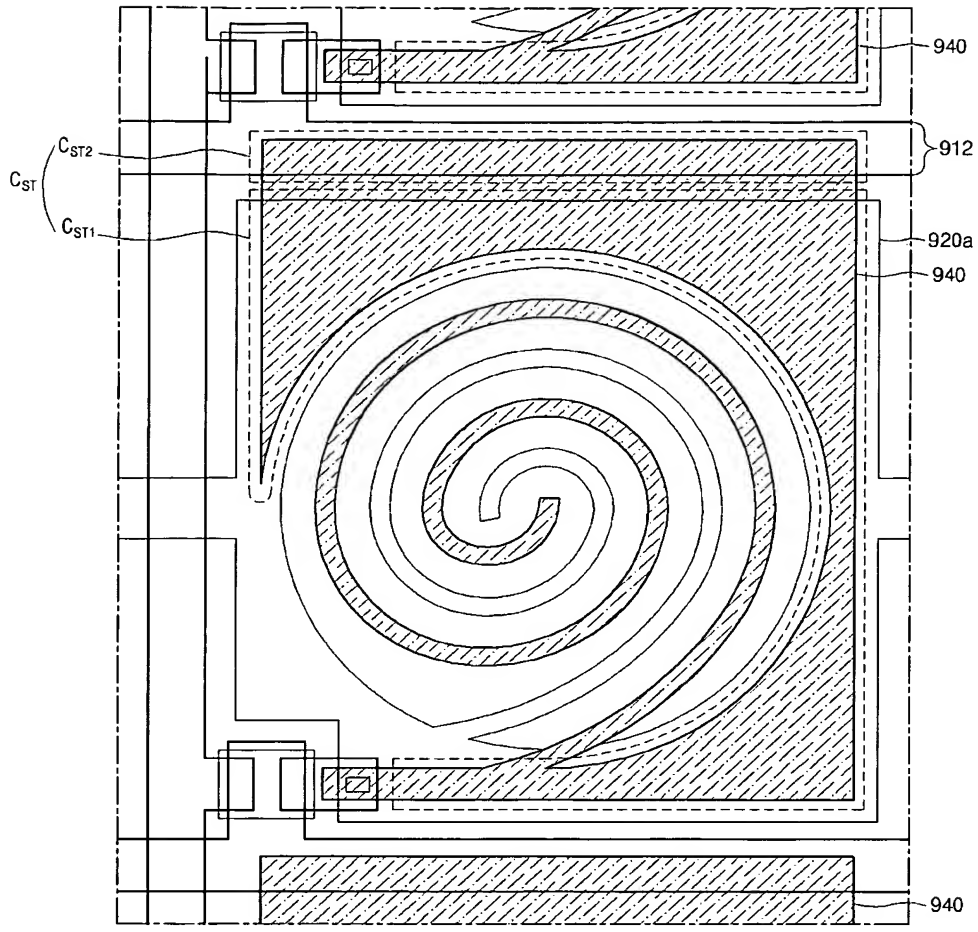
【FIG. 19】



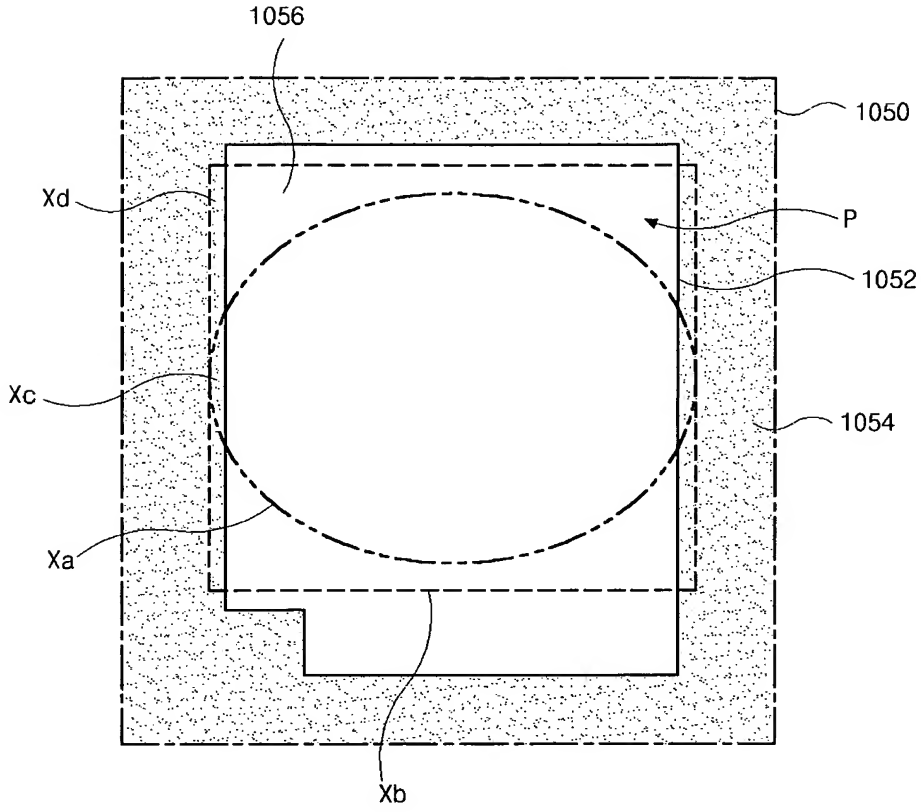
【FIG. 20】



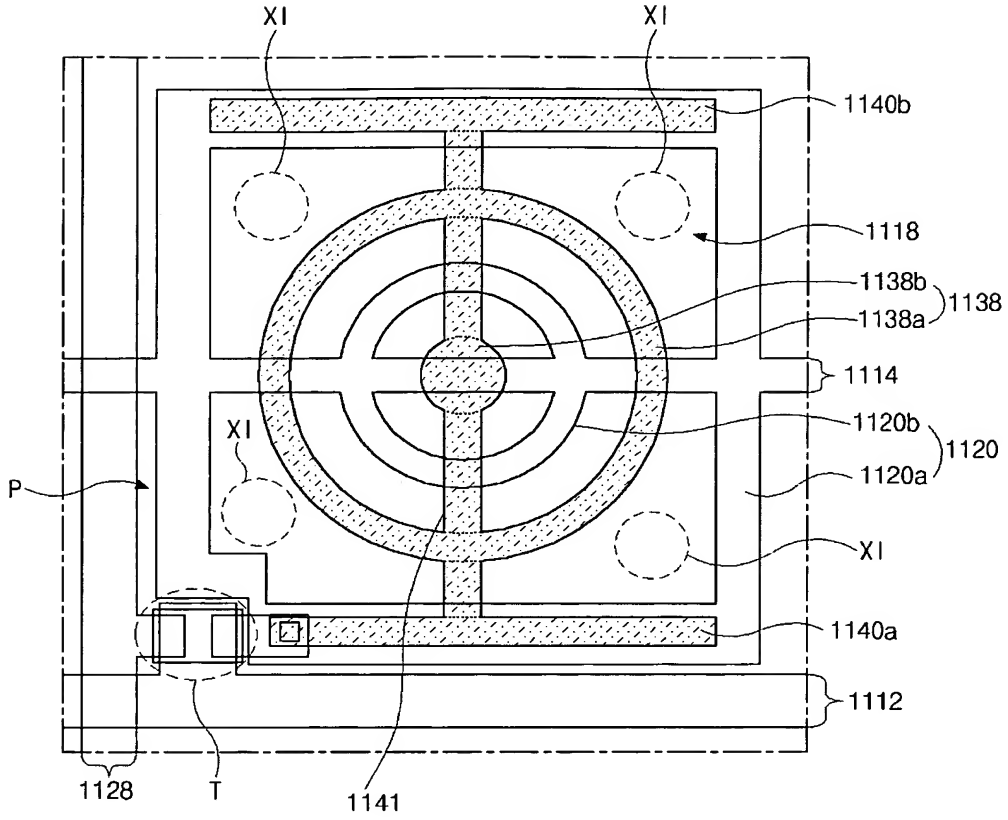
【FIG. 21】



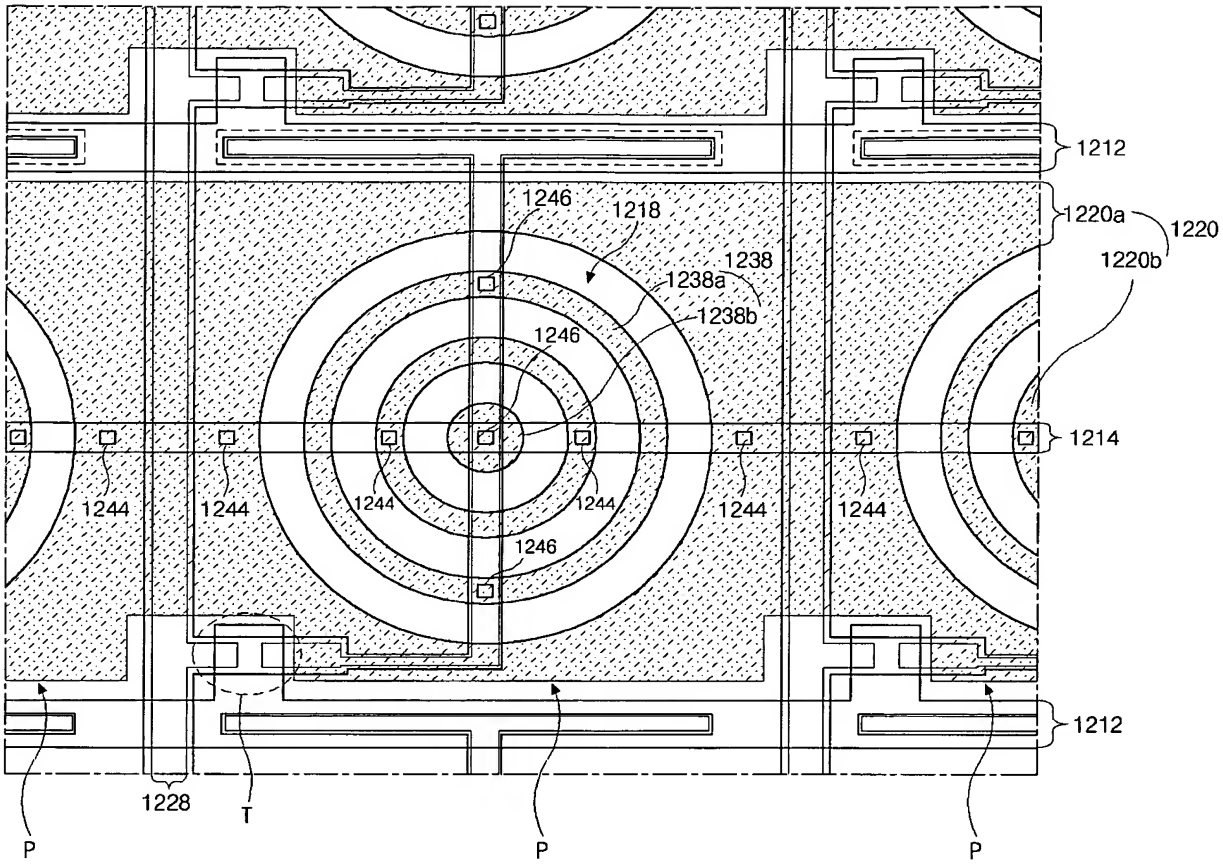
【FIG. 22】



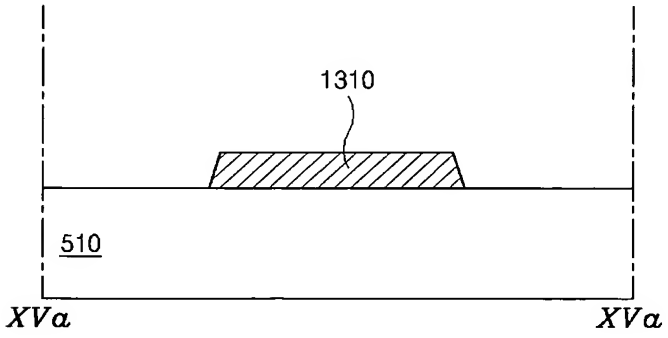
【FIG. 23】


XI
XI
1140b
1118
1138b
1138
1138a
1114
XI
1120b
1120
1120a
P
XI
1140a
1112
1128
T
1141

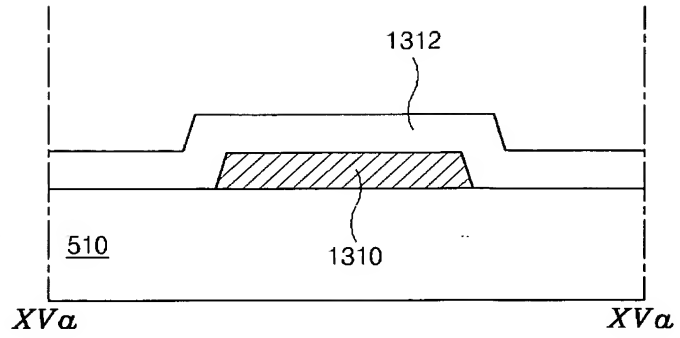
【FIG. 24】



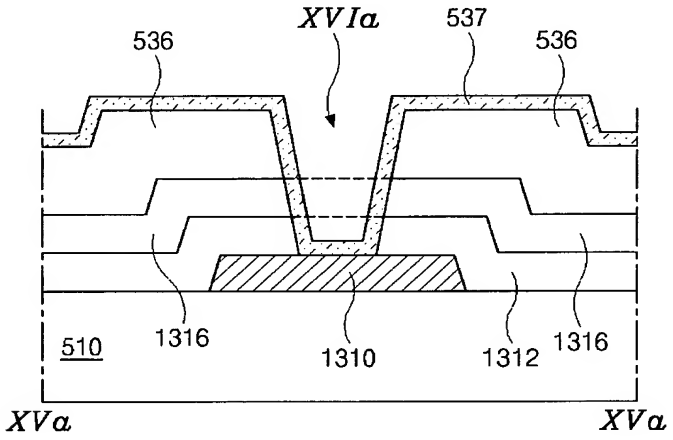
【FIG. 25A】



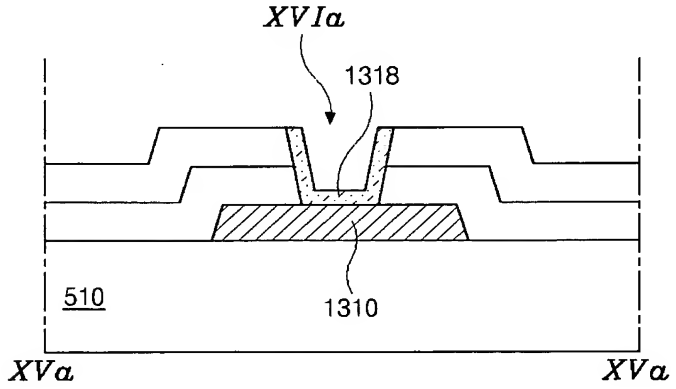
【FIG. 25B】



【FIG. 25C】

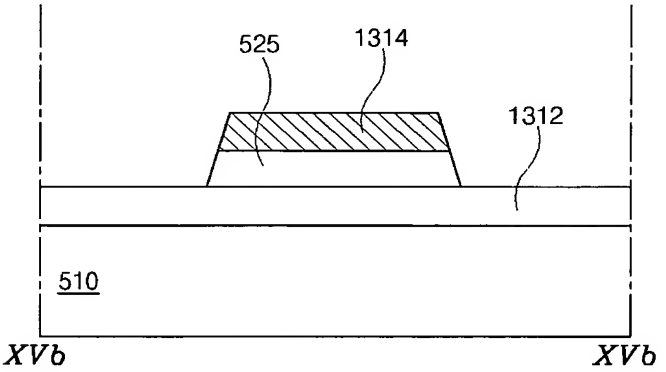


【FIG. 25D】

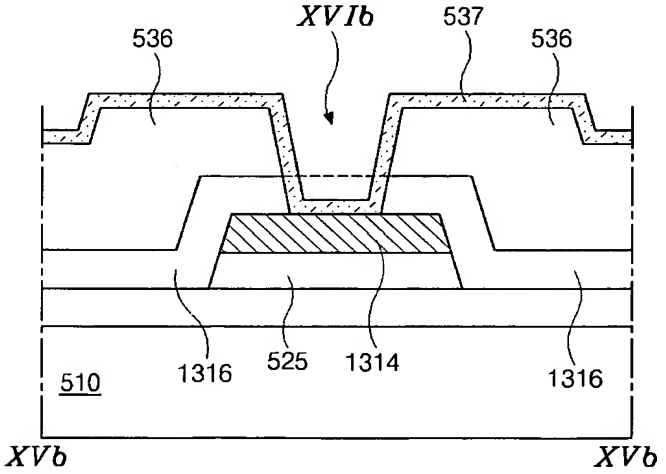


【FIG. 26A】

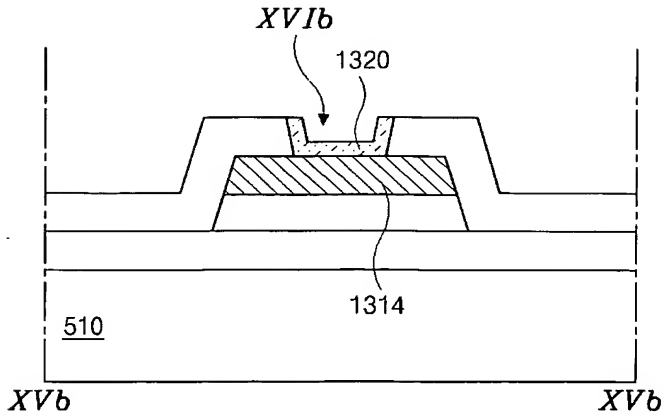
【FIG. 26B】



【FIG. 26C】



【FIG. 26D】


XVIb
1320
1314
510
XVb
XVb